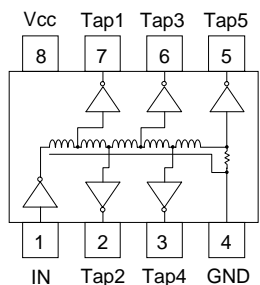


LVMDM Series LVC Low Voltage Logic Buffered 5-Tap Delay SMD Modules

Inputs accept voltages up to 5.5 V
74LVC type input can be driven from either 3.3V or 5V devices. This allows delay module to serve as a translator in a mixed 3.3V / 5V system environment.

- Low Profile 8-Pin Package Two Surface Mount Versions
- Low Voltage CMOS 74LVC Logic Buffered
- 5 Equal Delay Taps
- Operating Temp. -40°C to +85°C

LVMDM 8-Pin Schematic



Electrical Specifications at 25°C

LVC 5 Tap SMD P/N	Tap 1 (ns)	Tap 2 (ns)	Tap 3 (ns)	Tap 4 (ns)	Tap 5 (ns)	Tap-to-Tap (ns)
LVMDM-7G	3.0 ± 1.0	4.0 ± 1.0	5.0 ± 1.0	6.0 ± 1.0	7 ± 1.0	1.0 ± 0.4
LVMDM-9G	3.0 ± 1.0	4.5 ± 1.0	6.0 ± 1.0	7.5 ± 1.0	9 ± 1.0	1.5 ± 0.5
LVMDM-11G	3.0 ± 1.0	5.0 ± 1.0	7.0 ± 1.0	9.0 ± 1.0	11 ± 1.5	2.0 ± 0.6
LVMDM-13G	3.0 ± 1.0	5.5 ± 1.0	8.0 ± 1.0	10.5 ± 1.0	13 ± 1.5	2.5 ± 0.8
LVMDM-15G	3.0 ± 1.0	6.0 ± 1.0	9.0 ± 1.0	12.0 ± 1.5	15 ± 1.5	3.0 ± 1.0
LVMDM-20G	4.0 ± 1.0	8.0 ± 1.2	12.0 ± 1.5	16.0 ± 1.5	20 ± 2.0	4.0 ± 1.0
LVMDM-25G	5.0 ± 1.0	10.0 ± 1.5	15.0 ± 1.5	20.0 ± 2.0	25 ± 2.0	5.0 ± 1.5
LVMDM-30G	6.0 ± 1.0	12.0 ± 1.5	18.0 ± 1.5	24.0 ± 2.0	30 ± 2.0	6.0 ± 1.5
LVMDM-35G	7.0 ± 1.0	14.0 ± 1.5	21.0 ± 2.0	28.0 ± 2.0	35 ± 2.0	7.0 ± 1.8
LVMDM-40G	8.0 ± 1.0	16.0 ± 1.5	24.0 ± 2.0	32.0 ± 2.0	40 ± 2.0	8.0 ± 2.0
LVMDM-45G	9.0 ± 1.0	18.0 ± 1.5	27.0 ± 2.0	36.0 ± 2.0	45 ± 2.25	9.0 ± 2.0
LVMDM-50G	10.0 ± 1.5	20.0 ± 2.0	30.0 ± 2.0	40.0 ± 2.0	50 ± 2.5	10 ± 2.0
LVMDM-60G	12.0 ± 1.5	24.0 ± 2.0	36.0 ± 2.0	48.0 ± 2.4	60 ± 3.0	12 ± 2.0
LVMDM-75G	15.0 ± 2.0	30.0 ± 2.0	45.0 ± 2.25	60.0 ± 3.0	75 ± 3.75	15 ± 2.5
LVMDM-80G	16.0 ± 2.0	32.0 ± 2.0	48.0 ± 2.4	64.0 ± 3.2	80 ± 4.0	16 ± 2.5
LVMDM-100G	20.0 ± 2.0	40.0 ± 2.0	60.0 ± 3.0	80.0 ± 2.0	100 ± 5.0	20 ± 3.0

** These part numbers do not have 5 equal taps. Tap-to-Tap Delays reference Tap 1.

TEST CONDITIONS -- Low Voltage CMOS, LVC

- V_{CC} Supply Voltage 3.30VDC
 Input Pulse Voltage 2.70V
 Input Pulse Rise Time 3.0 ns max.
 Input Pulse Width / Period 1000 / 2000 ns
1. Measurements made at 25°C
 2. Delay Times measured at 1.50V level of leading edge.
 3. Rise Times measured from 0.75V to 2.40V.
 4. 50pf probe and fixture load on output under test.

OPERATING SPECIFICATIONS

- Supply Voltage, V_{CC} 3.3 ± 0.3 VDC
 Supply Current, I_{CC} 10 mA typ., 30 mA max.
 Supply Current, I_{CCL}: V_{IN} = GND 22 mA max.
 Supply Current, I_{CCH}: V_{IN} = V_{CC} 10 µA max.
 Input Voltage, V_I 0 V min., 5.5 V max.
 Logic "1" Input, V_{IH} 2.0 V min.
 Logic "0" Input, V_{IL} 0.8 V max.
 Logic "1" Out, V_{OH}: V_{CC} = 3V & I_{OH} = -24 mA 2.0 V min.
 Logic "0" Out, V_{OL}: V_{CC} = 3V & I_{OL} = 24 mA 0.55 V max.
 Input Capacitance, C_I 5 pF, typ.
 Input Pulse Width, P_{WI} 40% of Delay min.
 Operating Temperature Range -40° to +85°C
 Storage Temperature Range -65° to +150°C

P/N Description

LVMDM - XXX X

LVC Buffered 5 Tap Delay
Molded Package Series:

8-pin DIP: LVMDM

Total Delay in nanoseconds (ns)

Lead Style: Blank = Thru-hole
 G = "Gull Wing" SMD
 J = "J" Bend SMD

Examples: LVMDM-25G = 25ns (5ns per tap) 74LVC, 8-Pin G-SMD

LVMDM-100 = 100ns (20ns per tap) 74LVC, 8-Pin DIP

Dimensions in Inches (mm)

