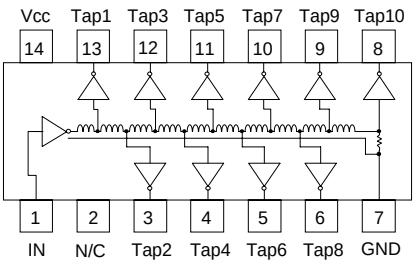
FAITD Series FAST / TTL Buffered 10-Tap Delay Modules

- *Low Profile 14-Pin Package Two Surface Mount Versions*
- *FAST/TTL Logic Buffered*
- *10 Equal Delay Taps*
- *Operating Temperature Range 0°C to +70°C*
- *Low Voltage CMOS Versions refer to LVITD Series*

FAITD Schematic



Electrical Specifications at 25°C

FAST 10 Tap 14-Pin P/N	Tap Delay Tolerances +/- 5% or 2ns (+/- 1ns <15ns)										Tap-to-Tap (ns)
	Tap 1	Tap 2	Tap 3	Tap 4	Tap 5	Tap 6	Tap 7	Tap 8	Tap 9	Total - Tap 10	
FAITD-12	3	4	5	6	7	8	9	10	11	12 ± 1.0	** 1.0 ± 0.5
FAITD-15	3	3.5	4.5	6	7.5	9	10.5	12	13.5	15 ± 1.0	** 1.5 ± 0.6
FAITD-20	3	4	6	8	10	12	14	16	18	20 ± 1.5	** 2.0 ± 0.7
FAITD-25	3	5	7.5	10	12.5	15	17.5	20	22.5	25 ± 2.0	** 2.5 ± 0.8
FAITD-30	3	6	9	12	15	18	21	24	27	30 ± 2.0	3.0 ± 1.0
FAITD-35	3.5	7	10.5	14	17.5	21	24.5	28	31.5	35 ± 2.0	3.5 ± 1.0
FAITD-40	4	8	12	16	20	24	28	32	36	40 ± 2.0	4.0 ± 1.0
FAITD-50	5	10	15	20	25	30	35	40	45	50 ± 2.5	5.0 ± 2.0
FAITD-60	6	12	18	24	30	36	42	48	54	60 ± 3.0	6.0 ± 2.0
FAITD-70	7	14	21	28	35	42	49	56	63	70 ± 3.5	7.0 ± 2.0
FAITD-75	7.5	15	22.5	30	37.5	45	52.5	60	67.5	75 ± 3.75	7.5 ± 2.0
FAITD-80	8	16	24	32	40	48	56	64	72	80 ± 4.0	8.0 ± 2.0
FAITD-100	10	20	30	40	50	60	70	80	90	100 ± 5.0	10 ± 2.0
FAITD-125	12.5	25	37.5	50	62.5	75	87.5	100	112.5	125 ± 6.25	12.5 ± 3.0
FAITD-150	15	30	45	60	75	90	105	120	135	150 ± 7.5	15 ± 3.0
FAITD-200	20	40	60	80	100	120	140	160	180	200 ± 10.0	20 ± 3.0
FAITD-250	25	50	75	100	125	150	175	200	225	250 ± 12.5	25 ± 3.0
FAITD-300	30	60	90	120	150	180	210	240	270	300 ± 15.0	30 ± 5.0
FAITD-500	50	100	150	200	250	300	350	400	450	500 ± 25.0	50 ± 6.0

** These part numbers do not have 5 equal taps. Tap-to-Tap Delays reference Tap 1.

TEST CONDITIONS -- FAST / TTL

V_{CC} Supply Voltage 5.00VDC
Input Pulse Voltage 3.20V
Input Pulse Rise Time ..... 3.0 ns max.
Input Pulse Width / Period ..... 1000 / 2000 ns

1. Measurements made at 25°C
2. Delay Times measured at 1.50V level of leading edge.
3. Rise Times measured from 0.75V to 2.40V.
4. 10pf probe and fixture load on output under test.

OPERATING SPECIFICATIONS

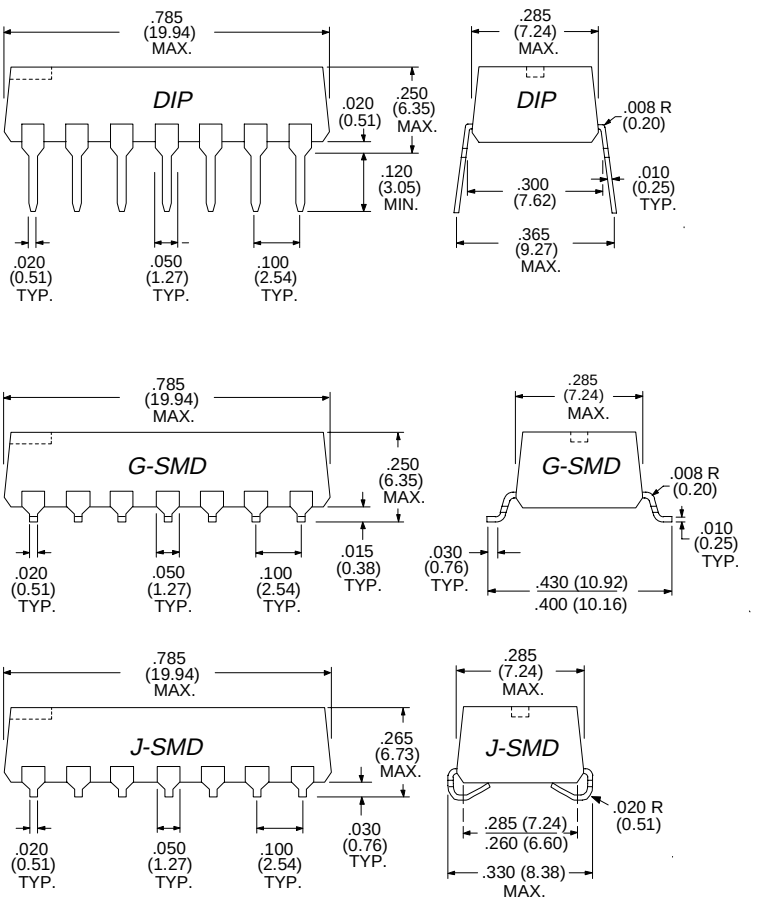
V_{CC} Supply Voltage ..... 5.00 ± 0.25 VDC
I_{CC} Supply Current ..... 25mA typ., 50 mA Max.
Logic "1" Input: V_{IH} ..... 2.00 V min., 5.50 V max.
I_{IH} ..... 20 µA max. @ 2.70V
Logic "0" Input: V_{IL} ..... 0.80 V max.
I_{IL} ..... -0.6 mA mA
V_{OH} Logic "1" Voltage Out ..... 2.40 V min.
V_{OL} Logic "0" Voltage Out ..... 0.50 V max.
P_{WI} Input Pulse Width ..... 20% of Delay min.
Operating Temperature Range ..... 0° to 70°C
Storage Temperature Range ..... -65° to +150°C

P/N Description ***FAITD - XXX X***

Buffered 10 Tap Delay
Molded Package Series:
14-pin DIP: FAITD
Total Delay in nanoseconds (ns)
Lead Style: Blank = Thru-hole
G = "Gull Wing" SMD
J = "J" Bend SMD

Examples: FAITD-75G = 75ns (7.5ns per tap)
74F, 14-Pin G-SMD
FAITD-100 = 100ns (10ns per tap)
74F, 14-Pin DIP

Dimensions in Inches (mm)



Specifications subject to change without notice. *For other values & Custom Designs, contact factory.* FAITD 9901

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