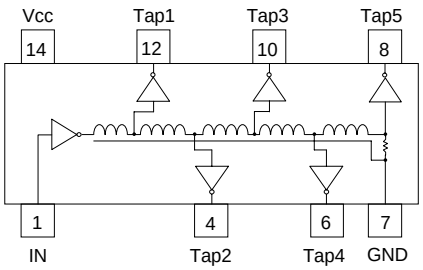
FAIDM Series FAST / TTL Buffered 5-Tap Delay Modules

- *Low Profile 14-Pin Package*
  Two Surface Mount Versions
- *FAST/TTL Logic Buffered*
- *5 Equal Delay Taps*
- *Operating Temperature*
  Range 0°C to +70°C
- *8-Pin Versions: FAMDM Series*
  SIP Versions: FSIDM Series
- *Low Voltage CMOS Versions*
  refer to LVMDM / LVIDM Series

FAIDM 14-Pin Schematic



Electrical Specifications at 25°C

FAST 5 Tap 14-Pin DIP P/N	Tap Delay Tolerances +/- 5% or 2ns (+/- 1ns <13ns)					Tap-to-Tap (ns)
	Tap 1	Tap 2	Tap 3	Tap 4	Total - Tap 5	
FAIDM-7	3.0	4.0	5.0	6.0	7 ± 1.0	** 1 ± 0.5
FAIDM-9	3.0	4.5	6.0	7.5	9 ± 1.0	** 1.5 ± 0.5
FAIDM-11	3.0	5.0	7.0	9.0	11 ± 1.0	** 2 ± 0.7
FAIDM-13	3.0	5.5	8.0	10.5	13 ± 1.5	** 2.5 ± 1.0
FAIDM-15	3.0	6.0	9.0	12.0	15 ± 1.5	3 ± 1.0
FAIDM-20	4.0	8.0	12.0	16.0	20 ± 2.0	4 ± 1.5
FAIDM-25	5.0	10.0	15.0	20.0	25 ± 2.0	5 ± 2.0
FAIDM-30	6.0	12.0	18.0	24.0	30 ± 2.0	6 ± 2.0
FAIDM-35	7.0	14.0	21.0	28.0	35 ± 2.0	7 ± 2.0
FAIDM-40	8.0	16.0	24.0	32.0	40 ± 2.0	8 ± 2.0
FAIDM-50	10.0	20.0	30.0	40.0	50 ± 2.5	10 ± 2.0
FAIDM-60	12.0	24.0	36.0	48.0	60 ± 3.0	12 ± 2.0
FAIDM-75	15.0	30.0	45.0	60.0	75 ± 3.75	15 ± 2.5
FAIDM-100	20.0	40.0	60.0	80.0	100 ± 5.0	20 ± 3.0
FAIDM-125	25.0	50.0	75.0	100.0	125 ± 6.25	25 ± 3.0
FAIDM-150	30.0	60.0	90.0	120.0	150 ± 7.5	30 ± 3.0
FAIDM-200	40.0	80.0	120.0	160.0	200 ± 10.0	40 ± 4.0
FAIDM-250	50.0	100.0	150.0	200.0	250 ± 12.5	50 ± 5.0
FAIDM-350	70.0	140.0	210.0	280.0	350 ± 17.5	70 ± 7.0
FAIDM-500	100.0	200.0	300.0	400.0	500 ± 25.0	100 ± 10.0

** These part numbers do not have 5 equal taps. Tap-to-Tap Delays reference Tap 1.

TEST CONDITIONS -- FAST / TTL

V_{CC} Supply Voltage 5.00VDC
Input Pulse Voltage 3.20V
Input Pulse Rise Time ..... 3.0 ns max.
Input Pulse Width / Period ..... 1000 / 2000 ns

1. Measurements made at 25°C
2. Delay Times measured at 1.50V level of leading edge.
3. Rise Times measured from 0.75V to 2.40V.
4. 10pf probe and fixture load on output under test.

OPERATING SPECIFICATIONS

V_{CC} Supply Voltage ..... 5.00 ± 0.25 VDC
I_{CC} Supply Current ..... 48 mA Maximum
Logic "1" Input: V_{IH} ..... 2.00 V min., 5.50 V max.
I_{IH} ..... 20 µA max. @ 2.70V
Logic "0" Input: V_{IL} ..... 0.80 V max.
I_{IL} ..... -0.6 mA mA
V_{OH} Logic "1" Voltage Out ..... 2.40 V min.
V_{OL} Logic "0" Voltage Out ..... 0.50 V max.
P_{WI} Input Pulse Width ..... 40% of Delay min.
Operating Temperature Range ..... 0° to 70°C
Storage Temperature Range ..... -65° to +150°C

P/N Description

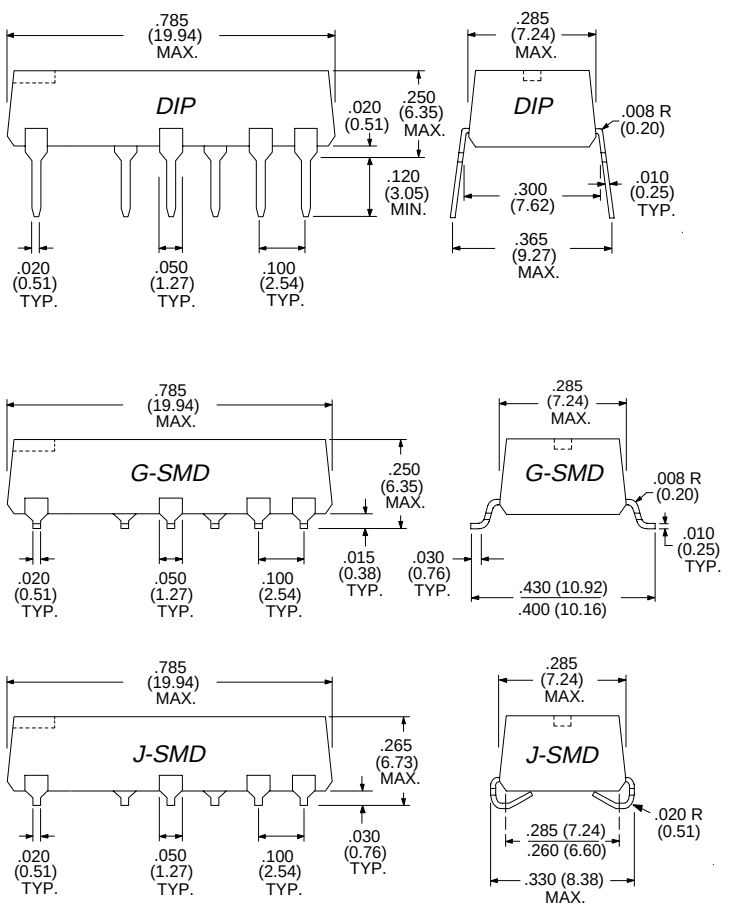
FAIDM - XXX X

Buffered 5 Tap Delay
Molded Package Series:
14-pin DIP: FAIDM
Total Delay in nanoseconds (ns)
Lead Style: Blank = Thru-hole
G = "Gull Wing" SMD
J = "J" Bend SMD

Examples: FAIDM-25G = 25ns (5ns per tap)
74F, 14-Pin G-SMD

FAIDM-100 = 100ns (20ns per tap)
74F, 14-Pin DIP

Dimensions in Inches (mm)



Specifications subject to change without notice. *For other values & Custom Designs, contact factory.* FAIDM 9901

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