10K / 10KH ECL Logic Pulse Width Control Modules

- Triggered by the input's rising edge (input pulse width 5 ns, min.), a pulse of specified width will be generated at the output
- High-to-low transitions will not trigger the unit.
- Propagation Delay of 2 ns typ., 4 ns max.
- 10K ECL ECLPWG Series: Designed for output duty-cycle less than 50%.
- 10KH ECL ECLHPW Series: Designed for output duty-cycle less than 65%.

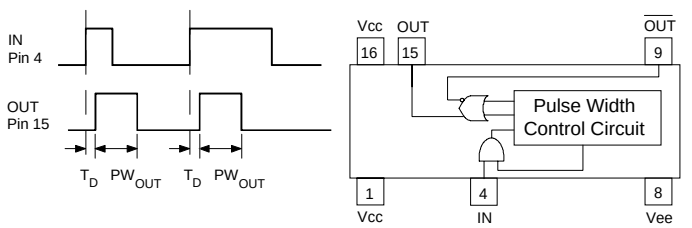
Electrical Specifications at 25°C

10K ECL Pulse Width Generator Modules		
Part Number	Maximum Freq. (MHz)	Output Pulse Width (ns)
ECLPWG-5	77.0	5 ± 1.00
ECLPWG-6	67.0	6 ± 1.00
ECLPWG-7	59.0	7 ± 1.00
ECLPWG-8	53.0	8 ± 1.00
ECLPWG-9	48.0	9 ± 1.00
ECLPWG-10	43.0	10 ± 1.50
ECLPWG-15	31.0	15 ± 2.00
ECLPWG-20	23.0	20 ± 2.00
ECLPWG-25	19.0	25 ± 2.00
ECLPWG-30	15.0	30 ± 2.00
ECLPWG-40	11.0	40 ± 2.00
ECLPWG-50	9.0	50 ± 2.50
ECLPWG-60	8.0	60 ± 3.00
ECLPWG-75	6.5	75 ± 3.75
ECLPWG-100	5.0	100 ± 5.00

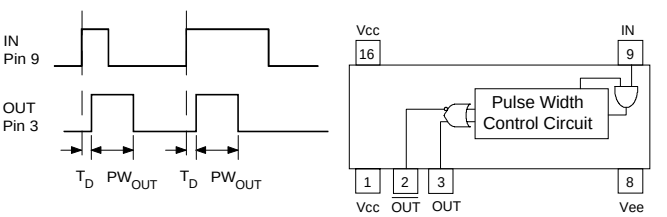
Electrical Specifications at 25°C

10KH ECL Pulse Width Generator Modules		
Part Number	Maximum Freq. (MHz)	Output Pulse Width (ns)
ECLHPW-5	100.0	5 ± 1.00
ECLHPW-6	98.0	6 ± 1.00
ECLHPW-7	88.0	7 ± 1.00
ECLHPW-8	84.0	8 ± 1.00
ECLHPW-9	68.0	9 ± 1.00
ECLHPW-10	56.0	10 ± 1.50
ECLHPW-15	41.0	15 ± 2.00
ECLHPW-20	30.0	20 ± 2.00
ECLHPW-25	23.0	25 ± 2.00
ECLHPW-30	20.0	30 ± 2.00
ECLHPW-40	15.0	40 ± 2.00
ECLHPW-50	12.7	50 ± 2.50
ECLHPW-60	10.6	60 ± 3.00
ECLHPW-75	8.2	75 ± 3.75
ECLHPW-100	6.3	100 ± 5.00

ECLPWG Schematic



ECLHPW Schematic

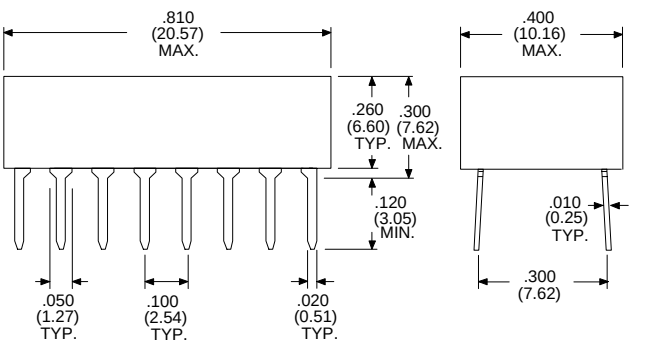


GENERAL: For Operating Specifications and Test Conditions, see Tables IV, V and VII on page 5 of this catalog. Delays specified for the Leading Edge.

Operating Temp. Range, **ECLPWG** ..... -40° to +85°C
Temperature Coefficient of PW ..... 300ppm/°C typical
Supply Current, I_{EE} , **ECLPWG** ..... 40 mA typ., 65 mA max.

Operating Temp. Range, **ECLHPW** ..... 0° to +75°C
Temperature Coefficient of PW ..... 300ppm/°C typical
Supply Current, I_{EE} , **ECLHPW** ..... 50 mA typ., 75 mA max.

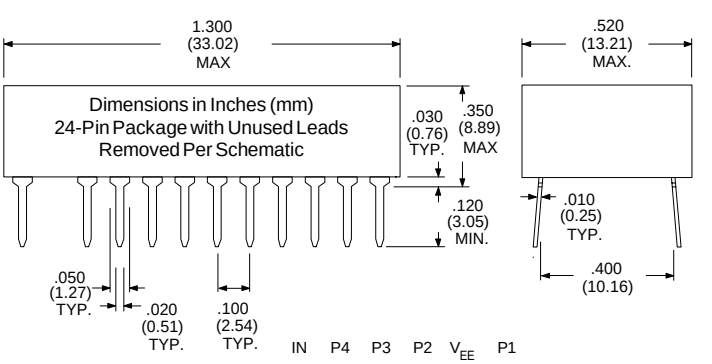
Dimensions in Inches (mm)
16-Pin Package with Unused Leads Removed Per Schematic



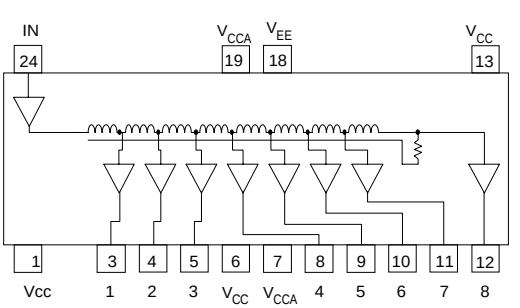
100K ECL Logic Delay Modules

Contact Factory for Data Sheets

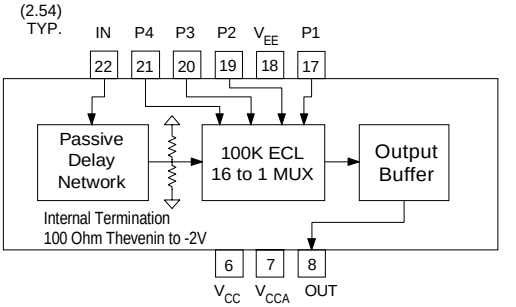
- *Buffered with 100K Series 300 Logic*
- *8 Equal Delay Taps Series: DDECL*
- *4-Bit Programmable Series: PPECL2*
- *Stable Delay vs. Temperature: 300 ppm/°C*
- *Operating Temperature Range 0°C to +85°C*



DDECL
8-Tap 100K
Schematic



PPECL2
4-Bit 100K
Schematic



Specifications subject to change without notice.

For other values & Custom Designs, contact factory.

ECLPW 1/98

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