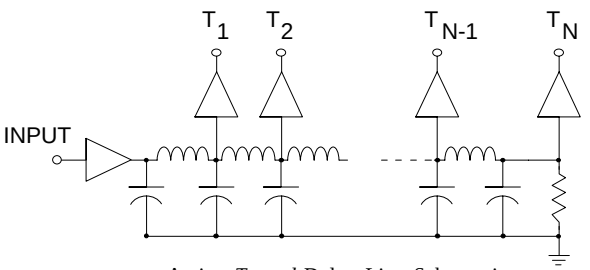
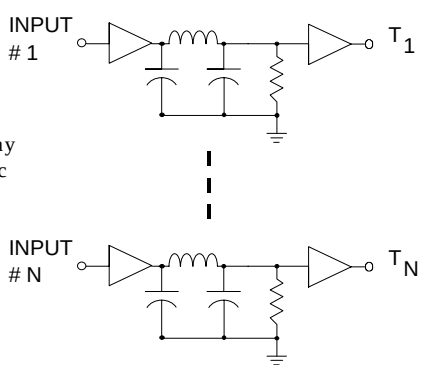
Logic Buffered Delay Modules

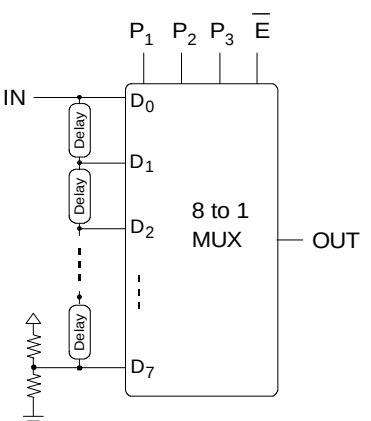
- *TTL - FAST - ECL - ACT CMOS Delays up to 1000ns*
- *5 & 10 Tap / Single / Dual / Triple and Quad Standard Footprints*
- *Gullwing & J Bend SMD Versions*
- *Programmables 3, 4, 5 & 6 Bit,*
- *Pulse Width Control & Gated Oscillators*
- *Customs ... Quick Turnaround*
- *Military Grade Versions Available*



Active *Tapped* Delay Line Schematic



Active *Multi*-Delay Schematic



Active *3-Bit Programmable* Delay Line Schematic

General: To avoid the difficulties associated with interfacing passive delay lines with digital integrated circuits, active delay lines have been developed to provide design flexibility and circuit simplification. Logic buffered input and outputs prevent the designer from having to contend with the loading issues of passive circuity, and the related output waveform transients. Unlike a passive delay line whose output rise time is proportional to its delay, the active line's output has the edge rate characteristic of the respective logic family. Similarly, the active delay modules will have the fan-in & fan-out ratings of that logic family. Thus, active delay lines can be used to drive a higher number of gates of a more complicated topology with minimal effect on signal quality or delay accuracy.

These devices will provide the Digital Design Engineer with simple modular solutions to a variety of timing requirements which commonly arise. Buffered Logic delay modules are ideally suited for situtations where the interval being considered is less than the period of the system clock, or where a precise timing adjustment is required. Also, by incorporating the functions of multiplexers or logic gates, active lines can perform as programmable delays, logic control delays, pulse-width control units and gated oscillators that will, in many applications, be capable of completely replacing complex gate arrangements.

These devices are of hybrid construction, combining Integrated Circuitry with Passive Networks utilizing inductive, capacitive, and resistive elements. Inputs & outputs are internally buffered and compensated for propagation delays and require no external components to perform their intended timing function (for ECL devices standard termination of Open Emitter-Follower Outputs is required).

All modules are designed to meet or exceed all applicable environmental requirements of MIL-D-83532, MIL-STD-883, and MIL-STD-202. Certain families available as MIL-GRADE by adding "M" suffix. Active delay lines are available in a wide variety of standard package configurations, for both through-hole and surface mount applications: "J" Style Surface Mount, Auto Insertable (DIP), Gull Wing Style Surface Mount, and Single-In-Line (SIP).

Minimum Pulse Width and BW Limitations: Although the output rise time of an active delay line is characteristic of its logic family, the bandwidth limitation is chiefly due to the rise and fall times of the internal delay network (see Rise time / BW notes for Passive Delays, pg. 2). This Low Pass Filter frequency limitation for active delay lines is expressed as a minimum pulse width that the delay line is guaranteed to pass. Reducing the input pulse width beneath this minimum typically results in shrinking output widths and eventually complete suppression. The most significant attenuation occurs at outputs with higher delay. Some degradation of the delay accuracy may occur near these limiting conditions, and we recommend that Delay Modules be evaluated under the intended operating conditions. There are options for increasing the effective bandwidth, and we encourage you to contact us regarding designs where minimum width is an issue.

Edge-to-Edge Relationship: Typically, active delay lines are specified for leading edge delay accuracy. This is a result of the physical switching properties of integrated circuits. For example, the logic "1" threshold of TTL devices is 2.0 Vdc minimum, at approximately 50% of the margin between the typical TTL low and high levels. However, to reach the TTL logic "0" threshold the negative-going pulse must drop down to 0.8 Vdc, or about 80% of the total signal amplitude. Because of this inherent asymmetry and its effect driving the internal delay circuit, the delay lines output pulse width will typically be less (2 to 3 ns) than the input pulse width. Rhombus has design variations that control delays for Leading and / or Trailing edges, and combinations of pulse polarity, width, and period.

Special Requirements: The listings in this catalog are necessarily limited to the most popular versions; intermediate values are readily available, simply contact the factory for data sheets and ordering information. Designs customized to your specific requirements and / or slight modifications to the existing products are welcome. Rhombus customarily provides most engineering services for first article samples at no charge. Please call one of our Applications Engineers today to discuss your requirement.

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