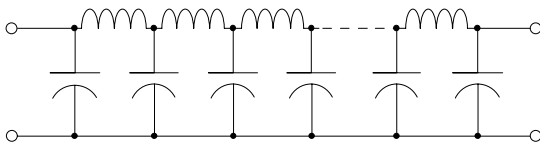


Delay Lines

Electromagnetic



- Low Distortion**
- Fast Rise Times**
- Single Output**
- 5 Taps**
- 10 Taps**
- 16 Taps**
- 20 Taps**
- Wide Range of Standard Family Impedances**

- 50 Ω**
- 75 Ω**
- 93 Ω**
- 100 Ω**
- 200 Ω**

Logic Buffered



- Buffered Input / Output**
- 5V FAST/TTL & Advanced CMOS**
- 3V Logic, Low Voltage CMOS**
- 10K & 10KH ECL**
- Single Output**
- 5 Taps**
- 10 Taps**
- Dual**
- Triple**
- Quad**
- Programmables**
- Special Function**
- Pulse Width Control**

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Founded in 1970, Rhombus Industries Incorporated is a privately owned corporation and a leading designer and manufacturer of transformers and magnetic products. Our headquarters is located in Huntington Beach, California and includes engineering, research

and development, complete manufacturing capabilities, marketing and extensive in-house environmental testing capabilities. Supporting the Huntington Beach facility is our privately owned and operated sub-assembly operation located in Thailand.

Insuring the accuracy, consistency, and overall quality of Rhombus products is of primary concern. All of our products are designed and built to meet the most demanding reliability requirements. We have an extensive quality control program which incorporates statistical process control and is also in strict compliance with MIL-I-45208.

For over 30 years, Rhombus has gained unique experience in providing quality components and innovative designs for users of magnetic products. Rhombus welcomes custom designs tailored to unique customer requirements. Our dedicated employees look forward to proving to you that Rhombus offers the price, delivery and application support advantages that can address your most critical needs.

For Downloadable Catalogs and Data Sheets, as well as Complete On-line Magnetic Product resources please visit us on the web at

www.rhombus-ind.com

Cross Reference

Application Notes

Part Index

with links to data sheets

I.C. Guide

Inductor Selction Guide

CM Choke Guide

Sales Representatives

Catalogs

Transformers (Datacomm) Catalog

Mag. Compontents (Power/SMPS) Catalog

Audio Magnetics Catalog

Delay Line Catalog

June 2001

Delay Lines

Passive & Logic Buffered

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10 Tap 14-Pin DIL <i>TZB</i>	7
5 Tap 7-Pin SIP <i>SIP4</i>	8
10 Tap 14-Pin SIP <i>SIP5</i>	8
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Passive Delay Line Design Considerations

A Passive Delay Line is a special purpose Low Pass Filter designed to delay (phase shift) the input signal by a specified increment of time, and is composed of series inductors and shunt capacitors with values dictated by the line impedance.

Design: This LC network may be used to pass either analog or digital signals whose bandwidth is compatible with the intended range of operation for the delay line. A specific delay and impedance, determine the required LC values of the network:

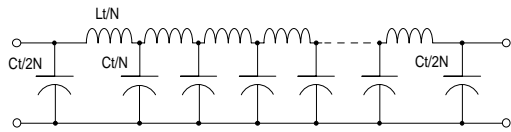


Figure 1A. Passive Delay Line Schematic Diagram.

$$T_d = \sqrt{(L_t \times C_t)}$$

T_d = Total Delay (ns)

Z_o = Impedance (Ohms)

L_t = Total Line Inductance (μ H)

C_t = Total Line Capacitance (pF)

$$Z_o = \sqrt{(L_t / C_t)}$$

Rise Time: The rise time of a delay line is typically measured from the 10% to 90% points of the leading edge of the output pulse. The measured output risetime (t_o) is a function of the input rise time (t_i) and the true rise time of the delay line (t_r):

$$t_r = \sqrt{t_o^2 - t_i^2}$$

An analog delay line's bandwidth (-3dB attenuation) is related to the network's rise time which is dependent upon the total number (N) of LC sections. The delay-to-rise time ratio is the figure of merit, or Quality Factor, used to characterize delay lines. Generally, the greater figure of merit implies higher number of sections, and therefore higher cost. The bandwidth for the network, and number of sections follow these approximations:

$$BW \approx .35 / t_r \quad N \approx (T_d / t_r)^{1.36}$$

Attenuation: The output voltage attenuation of a delay line has several contributing factors:

1. Internal D.C. resistance (DCR)
2. Dielectric and ground plane losses
3. Loading effects at taps
4. Impedance mismatches at terminations
5. Frequency limitations (BW) of delay line

When the delay line is minimally loaded, properly terminated and the input pulse widths are significantly greater than the line's rise time, attenuation is given by:

$$\text{Attenuation (\%)} = 1 - (Z_o / (Z_o + DCR))$$

Series Connection: Passive delay lines of the same impedance can be connected input-to-output (cascaded) to optimize rise time and/or obtain specific delay values. Termination is required only at the output of the final stage. The rise time of the grouped lines is given by

$$t_o = \sqrt{t_i^2 + t_{r1}^2 + t_{r2}^2 + \dots + t_{rN}^2}$$

Reflections: Loading at taps should be at least 10 times the characteristic impedance to minimize reflections due to transmission line effects. The reflected voltage due to a tap loaded by a resistance, R_L , is given by

$$\text{Reflection (\%)} = 1 - (1 / (1 + Z_o/2R_L))$$

In certain applications, mismatches can be used to achieve pulse-shaping requirements.

Reflections, continued: There are three basic rules relating to reflections in passive delay line applications:

- 1) No reflections at either terminal of a line which is terminated with its characteristic impedance.

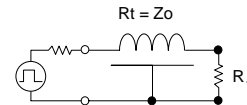


Figure 2A.

- 2) A reflection, equal in amplitude and of same polarity to the impinging signal, will occur at the input of a line which is open circuited. ($R_t = \text{infinite}$, see figures below.)

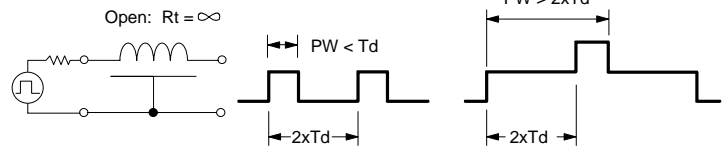


Figure 3A.

- 3) A reflection, equal in amplitude and of opposite polarity to the impinging signal, will occur at the input of a line which is short circuited. ($R_t = 0$, see figures below.)

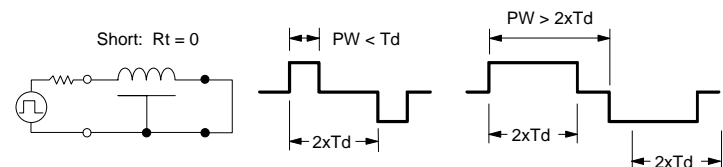


Figure 4A.

Circuit Considerations: To assure delay accuracy and prevent signal distortion, care should be taken to properly integrate the passive delay line into the circuit design. A board trace can load a tap with several picofarads of capacitance which will increase delay, rise time, distortion and attenuation. The designer should calculate inductance and capacitance values of the delay line (L_t , C_t) to determine if anticipated board loading is significant. For typical passive delay line applications, the following design criteria provide optimum performance:

1. The line should be properly terminated.
2. Minimize tap loading. $10 \times Z_o$ min. recommended.
3. Minimize trace lengths to delay line.
4. Circuit should have massive ground plane.
5. All common connections should be used.

We encourage you to call and discuss the details of your design with one of our application engineers. We offer quick turnaround on samples, and custom versions are available, generally at no cost for existing package configurations.

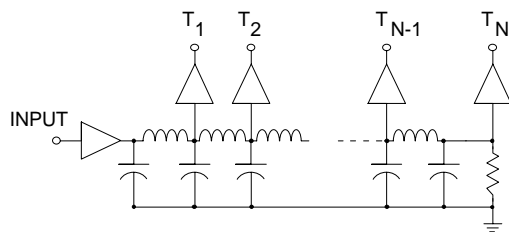
Operating Specifications - Passive Delay Lines

Pulse Overshoot (Pos)	5% to 10%, typical
Pulse Distortion (S)	3% typical
Working Voltage	25 VDC maximum
Dielectric Strength	100VDC minimum
Insulation Resistance	1,000 M Ω min. @ 100VDC
Temperature Coefficient	70 ppm/ $^{\circ}$ C, typical
Bandwidth (f_c)	$0.35/t_r$ approx.
Operating Temperature Range	-55° to $+125^{\circ}$ C
Storage Temperature Range	-65° to $+150^{\circ}$ C

Logic Buffered Delay Module Design Considerations

- Delays up to 1000ns
- 5 & 10 Tap Modules
- Gated Oscillator Modules
- 5V -- TTL / FAST, ACT CMOS
- Single / Dual / Triple / Quad
- DIP, Gullwing & J Bend SMD
- 3V -- Low Voltage CMOS, LVC, AC
- Programmables 3, 4, 5 & 6 Bit
- Military Grade Versions Available
- 10K & 10KH ECL
- Pulse Width Control
- Customs available ... Quick Delivery

General: To avoid the difficulties associated with interfacing passive delay lines with digital integrated circuits, active delay lines have been developed to provide design flexibility and circuit simplification. Logic buffered input and outputs prevent the designer from having to contend with the loading issues of passive circuitry, and the related output waveform transients. Unlike a passive delay line whose output rise time is proportional to its delay, the active line's output has the edge rate characteristic of the respective logic family. Similarly, the active delay modules will have the fan-in & fan-out ratings of that logic family. Thus, active delay lines can be used to drive a higher number of gates of a more complicated topology with minimal effect on signal quality or delay accuracy.



Active Tapped Delay Line Schematic

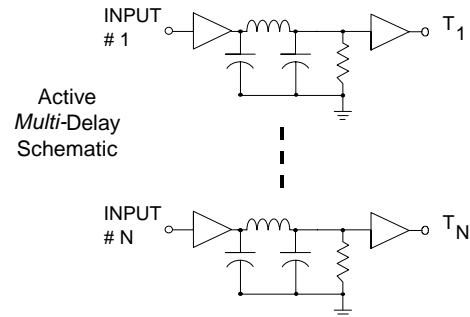
These devices will provide the Digital Design Engineer with simple modular solutions to a variety of timing requirements which commonly arise. Buffered Logic delay modules are ideally suited for situations where the interval being considered is less than the period of the system clock, or where a precise timing adjustment is required. Also, by incorporating the functions of multiplexers or logic gates, active lines can perform as programmable delays, logic control delays, pulse-width control units and gated oscillators that will, in many applications, be capable of completely replacing complex gate arrangements.

These devices are of hybrid construction, combining Integrated Circuitry with Passive Networks utilizing inductive, capacitive, and resistive elements. Inputs & outputs are internally buffered and compensated for propagation delays and require no external components to perform their intended timing function (for ECL devices standard termination of Open Emitter-Follower Outputs is required).

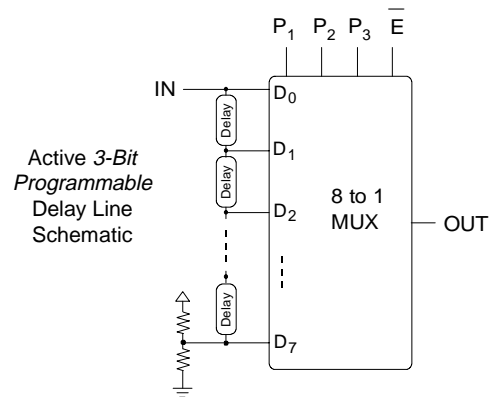
All modules are designed to meet or exceed all applicable environmental requirements of MIL-D-83532, MIL-STD-883, and MIL-STD-202. Certain families available as MIL-GRADE by adding "M" suffix. Active delay lines are available in a wide variety of standard package configurations, for both through-hole and surface mount applications: "J" Style Surface Mount, Auto Insertable (DIP), Gull Wing Style Surface Mount, and Single-In-Line (SIP).

Minimum Pulse Width and BW Limitations: Although the output rise time of an active delay line is characteristic of its logic family, the bandwidth limitation is chiefly due to the rise and fall times of the internal delay network (see Rise time / BW notes for Passive Delays, pg. 2). This Low Pass Filter frequency limitation for active delay lines is expressed as a minimum pulse width that the delay line is guaranteed to pass. Reducing the input pulse width beneath this minimum typically results in shrinking output widths and eventually complete suppression.

Min. PW and BW Limitations, continued: The most significant attenuation occurs at outputs with higher delay. Some degradation of the delay accuracy may occur near these limiting conditions, and we recommend that Delay Modules be evaluated under the intended operating conditions. There are options for increasing the effective bandwidth, and we encourage you to contact us regarding designs where minimum width is an issue.



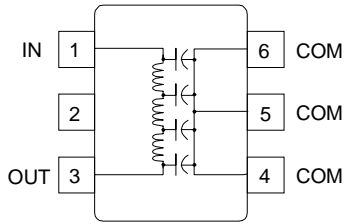
Edge-to-Edge Relationship: Typically, active delay lines are specified for leading edge delay accuracy. This is a result of the physical switching properties of integrated circuits. For example, the logic "1" threshold of TTL devices is 2.0 Vdc minimum, at approximately 50% of the margin between the typical TTL low and high levels. However, to reach the TTL logic "0" threshold the negative-going pulse must drop down to 0.8 Vdc, or about 80% of the total signal amplitude. Because of this inherent asymmetry and its effect driving the internal delay circuit, the delay lines output pulse width will typically be less (2 to 3 ns) than the input pulse width. Rhombus has design variations that control delays for Leading and/or Trailing edges, and combinations of pulse polarity, width, and period.



Special Requirements: The listings in this catalog are necessarily limited to the most popular versions; intermediate values are readily available, simply contact the factory for data sheets and ordering information. Designs customized to your specific requirements and/or slight modifications to the existing products are welcome. Rhombus customarily provides most engineering services for first article samples at no charge. Please call one of our Applications Engineers today to discuss your requirement.

SH6G Series Mini 6-Pin SMD Passive Delay Modules

SH6G Schematic

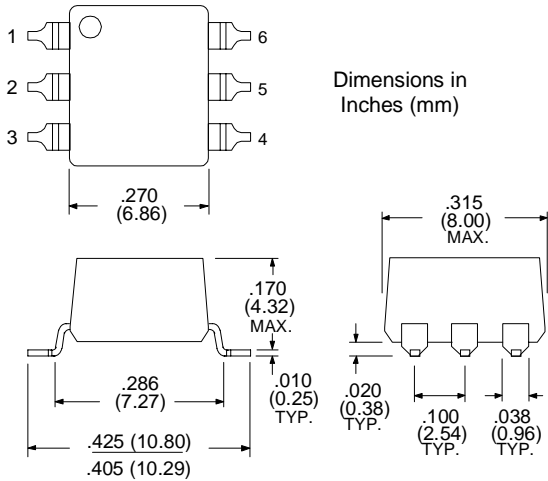


- Low Distortion LC Network
- Stable Delay vs. Temperature: 100 ppm/°C
- Operating Temperature Range -55°C to +125°C
- Standard Impedances: 50, 75, 100 Ω
For other impedances (up to 500Ω) visit web page or contact factory
- DIP version available: SH6D Series

Electrical Specifications at 25°C ^{1,2,3,4}

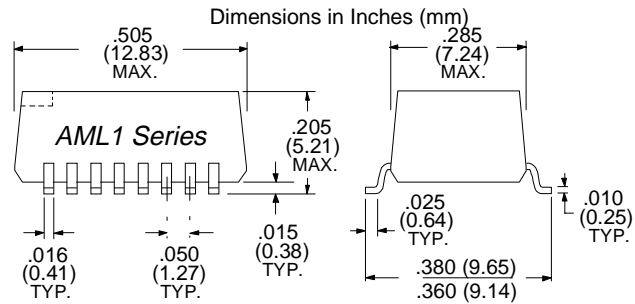
Delay (ns)	Rise Time 10%-90% max. (ns)	DCR max. (Ohms)	50 Ohm Part Number	75 Ohm Part Number	100 Ohm Part Number
1.0 ± .20	0.70	0.35	SH6G-0105	SH6G-0107	SH6G-0101
1.5 ± .20	0.80	0.35	SH6G-0155	SH6G-0157	SH6G-0151
2.0 ± .20	0.90	0.35	SH6G-0205	SH6G-0207	SH6G-0201
2.5 ± .25	1.00	0.40	SH6G-0255	SH6G-0257	SH6G-0251
3.0 ± .30	1.20	0.40	SH6G-0305	SH6G-0307	SH6G-0301
4.0 ± .40	1.50	0.45	SH6G-0405	SH6G-0407	SH6G-0401
5.0 ± .40	1.80	0.50	SH6G-0505	SH6G-0507	SH6G-0501
6.0 ± .40	2.20	0.55	SH6G-0605	SH6G-0607	SH6G-0601
7.0 ± .40	2.40	0.55	SH6G-0705	SH6G-0707	SH6G-0701
7.5 ± .40	2.50	0.60	SH6G-0755	SH6G-0757	SH6G-0751
8.0 ± .40	2.60	0.75	SH6G-0805	SH6G-0807	SH6G-0801
9.0 ± .50	2.80	0.75	SH6G-0905	SH6G-0907	SH6G-0901
10.0 ± .60	3.00	0.80	SH6G-1005	SH6G-1007	SH6G-1001
12.0 ± .60	3.30	0.85	SH6G-1105	SH6G-1107	SH6G-1101

1. Rise Times are measured 20% to 80% points.
2. Delay Times measured at 50% points of leading edge.
3. Impedance, Z_o, tolerance ± 10 %
4. Output terminated to ground through R_L = Z_o

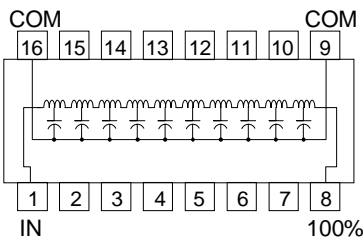


AML1 Series Mini 16-Pin 50-mil SMD Passive Delay Modules

- Low Distortion LC Network
- Stable Delay vs. Temperature: 100 ppm/°C
- Operating Temp. Range -55°C to +125°C
- Standard Impedances: 50, 75, 100 Ω
For other impedances (up to 500Ω) visit web page or contact factory



AML1 Schematic



Electrical Specifications at 25°C ^{1,2,3,4} (refer to Notes 1-4 above)

Delay (ns)	Rise Time 20% - 80% max. (ns)	DCR max. (Ohms)	50 Ohm Part Number	75 Ohm Part Number	100 Ohm Part Number	200 Ohm Part Number
1.0 ± .20	1.6	.20	AML1-1-50	AML1-1-75	AML1-1-10	AML1-1-20
1.5 ± .20	1.6	.30	AML1-1P5-50	AML1-1P5-75	AML1-1P5-10	AML1-1P5-20
2.0 ± .20	1.6	.40	AML1-2-50	AML1-2-75	AML1-2-10	AML1-2-20
2.5 ± .20	1.6	.50	AML1-2P5-50	AML1-2P5-75	AML1-2P5-10	AML1-2P5-20
3.0 ± .20	1.7	.60	AML1-3-50	AML1-3-75	AML1-3-10	AML1-3-20
4.0 ± .20	1.7	.70	AML1-4-50	AML1-4-75	AML1-4-10	AML1-4-20
5.0 ± .25	1.8	.80	AML1-5-50	AML1-5-75	AML1-5-10	AML1-5-20
6.0 ± .30	2.0	.85	AML1-6-50	AML1-6-75	AML1-6-10	AML1-6-20
7.0 ± .30	2.2	.90	AML1-7-50	AML1-7-75	AML1-7-10	AML1-7-20
8.0 ± .30	2.4	.95	AML1-8-50	AML1-8-75	AML1-8-10	AML1-8-20
9.0 ± .30	2.6	1.10	AML1-9-50	AML1-9-75	AML1-9-10	AML1-9-20
10 ± .30	2.8	1.20	AML1-10-50	AML1-10-75	AML1-10-10	AML1-10-20
12 ± .50	3.2	1.50	AML1-12-50	AML1-12-75	AML1-12-10	AML1-12-20
15 ± .70	3.8	1.70	AML1-15-50	AML1-15-75	AML1-15-10	AML1-15-20
20 ± 1.0	4.8	2.00	AML1-20-50	AML1-20-75	AML1-20-10	AML1-20-20

Specifications subject to change without notice.

For other values & Custom Designs, contact factory.

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TEL: (714) 898-0960

FAX: (714) 896-0971

AMZ & AMY Series Passive 5-Tap DIP/SMD Delay Modules

- Low Profile 8-Pin Package for Surface Mount Applications
- Low Distortion LC Network
- 5 Equal Delay Taps
- Fast Rise Time -- $BW \approx 0.35 / t_r$
- Standard Impedances: 50 - 75 - 100 - 200 Ω
- Stable Delay vs. Temperature: 100 ppm/ $^{\circ}C$
- Operating Temperature Range -55 $^{\circ}C$ to +125 $^{\circ}C$

Operating Specifications - Passive Delay Lines

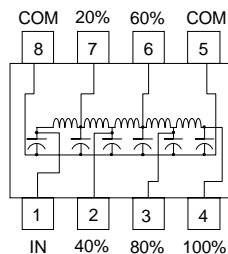
Pulse Overshoot (Pos)	5% to 10%, typical
Pulse Distortion (S)	3% typical
Working Voltage	25 VDC maximum
Dielectric Strength	100VDC minimum
Insulation Resistance	1,000 M Ω min. @ 100VDC
Temperature Coefficient	70 ppm/ $^{\circ}C$, typical
Bandwidth (f_c)	0.35/ t_r approx.
Operating Temperature Range	-55 $^{\circ}$ to +125 $^{\circ}C$
Storage Temperature Range	-65 $^{\circ}$ to +150 $^{\circ}C$

Electrical Specifications at 25 $^{\circ}C$ ^{1,2,3} Note: For SMD Package add "G" of "J" as below to P/N in Table

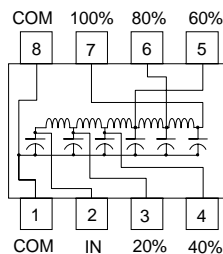
Delay Tolerances		50 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	75 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	100 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	200 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)
Total (ns)	Tap-to-Tap (ns)												
2.5 \pm 0.3	0.5 \pm 0.2	AMZ-2.55	1.5	0.4	AMZ-2.57	1.5	0.6	AMZ-2.51	1.5	0.6	AMZ-2.52	1.5	0.9
5 \pm 0.5	1.0 \pm 0.3	AMZ-5.55	2.0	0.5	AMZ-5.57	2.0	0.6	AMZ-5.51	2.0	0.6	AMZ-5.52	2.0	1.1
6 \pm 0.5	1.2 \pm 0.4	AMZ-6.55	2.3	0.5	AMZ-6.57	2.3	0.6	AMZ-6.51	2.4	0.7	AMZ-6.52	2.6	1.1
7 \pm 0.5	1.4 \pm 0.4	AMZ-7.55	2.6	0.6	AMZ-7.57	2.6	0.6	AMZ-7.51	2.8	0.8	AMZ-7.52	2.8	1.1
7.5 \pm 0.5	1.5 \pm 0.5	AMZ-7.55	2.8	0.6	AMZ-7.57	2.8	0.8	AMZ-7.51	2.9	0.8	AMZ-7.52	2.9	1.4
8 \pm 0.5	1.6 \pm 0.5	AMZ-8.55	3.0	0.6	AMZ-8.57	3.0	0.9	AMZ-8.51	3.0	0.8	AMZ-8.52	3.1	1.4
9 \pm 0.5	1.8 \pm 0.5	AMZ-9.55	3.3	0.7	AMZ-9.57	3.4	0.9	AMZ-9.51	3.4	0.8	AMZ-9.52	3.4	1.4
10 \pm 1.0	2.0 \pm 0.5	AMZ-10.55	3.4	0.7	AMZ-10.57	3.5	0.9	AMZ-10.51	3.6	0.9	AMZ-10.52	3.6	1.6
15 \pm 1.0	3.0 \pm 0.6	AMZ-15.55	5.2	0.9	AMZ-15.57	5.2	1.7	AMZ-15.51	5.2	1.8	AMZ-15.52	5.2	2.7
20 \pm 1.0	4.0 \pm 1.0	AMZ-20.55	6.8	1.0	AMZ-20.57	6.8	1.9	AMZ-20.51	6.8	2.0	AMZ-20.52	6.8	2.8
25 \pm 1.25	5.0 \pm 1.0	AMZ-25.55	8.5	1.3	AMZ-25.57	8.5	2.1	AMZ-25.51	8.5	2.2	AMZ-25.52	8.5	3.0
30 \pm 1.5	6.0 \pm 1.5	AMZ-30.55	10.2	1.4	AMZ-30.57	10.2	2.2	AMZ-30.51	10.2	2.4	AMZ-30.52	10.2	3.2
35 \pm 1.75	7.0 \pm 1.5	AMZ-35.55	11.9	1.5	AMZ-35.57	11.9	2.4	AMZ-35.51	11.9	2.6	AMZ-35.52	11.9	3.4
40 \pm 2.0	8.0 \pm 1.8	AMZ-40.55	13.6	1.6	AMZ-40.57	13.6	2.7	AMZ-40.51	13.6	2.8	AMZ-40.52	13.6	3.6
50 \pm 2.5	10.0 \pm 2.0	AMZ-50.55	17.0	2.0	AMZ-50.57	17.0	2.9	AMZ-50.51	17.0	3.1	AMZ-50.52	17.0	5.5
60 \pm 3.0	12.0 \pm 2.5	AMZ-60.55	20.4	2.2	AMZ-60.57	20.4	3.3	AMZ-60.51	20.4	3.3	AMZ-60.52	20.4	6.2
75 \pm 3.75	15.0 \pm 3.0	AMZ-75.55	25.5	2.5	AMZ-75.57	25.5	3.6	AMZ-75.51	25.5	3.6	AMZ-75.52	25.5	6.8
80 \pm 4.0	16.0 \pm 3.0	AMZ-80.55	27.2	2.6	AMZ-80.57	27.2	3.4	AMZ-80.51	27.2	5.0	AMZ-80.52	27.2	7.0
100 \pm 5.0	20.0 \pm 3.0	AMZ-100.55	34.0	3.0	AMZ-100.57	34.0	3.7	AMZ-100.51	34.0	5.8	AMZ-100.52	34.0	7.8

1. Rise Times are measured from 10% to 90% points.
2. Delay Times measured at 50% point of leading edge.
3. Output (100% Tap) terminated to ground through $R_L = Z_0$.

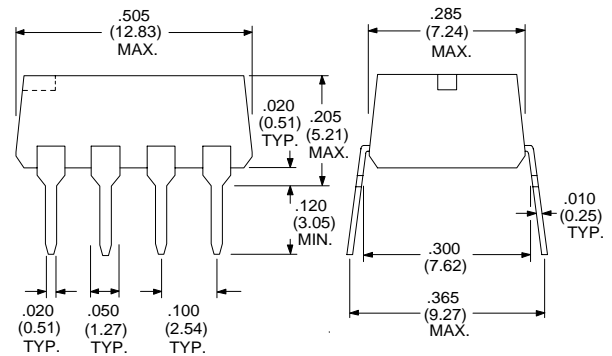
AMZ Style Schematic Recommended for New Designs



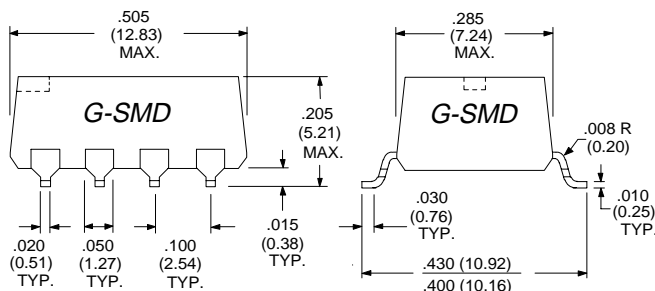
AMY Style Schematic Per table, substitute AMY for AMZ in P/N



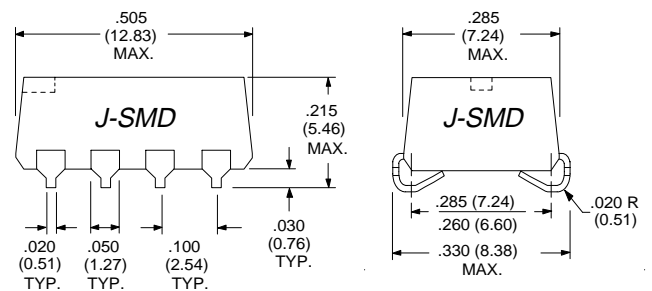
Dimensions in Inches (mm)



To Specify SMD: Add Suffix "G" to P/N



To Specify SMD: Add Suffix "J" to P/N



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AIZ Series Passive 10-Tap DIP/SMD Delay Modules

- Low Profile 14-Pin Package
DIP & Surface Mount Versions
- Low Distortion LC Network
- 10 Equal Delay Taps, Variety of Footprints
- Fast Rise Time -- $BW \approx 0.35 / t_r$
- Standard Impedances: 50 - 75 - 100 - 200 Ω
- Stable Delay vs. Temperature: 100 ppm/ $^{\circ}C$
- Operating Temperature Range -55 $^{\circ}C$ to +125 $^{\circ}C$

- Operating Specifications - *Passive Delay Lines*
- Pulse Overshoot (Pos) 5% to 10%, typical
 - Pulse Distortion (S) 3% typical
 - Working Voltage 25 VDC maximum
 - Dielectric Strength 100VDC minimum
 - Insulation Resistance 1,000 M Ω min. @ 100VDC
 - Temperature Coefficient 70 ppm/ $^{\circ}C$, typical
 - Bandwidth (f_c) 0.35/ t_r approx.
 - Operating Temperature Range -55 $^{\circ}$ to +125 $^{\circ}C$
 - Storage Temperature Range -65 $^{\circ}$ to +150 $^{\circ}C$

Electrical Specifications at 25 $^{\circ}C$ ^{1,2,3} Note: For Gullwing SMD Package add "G" to P/N in Table

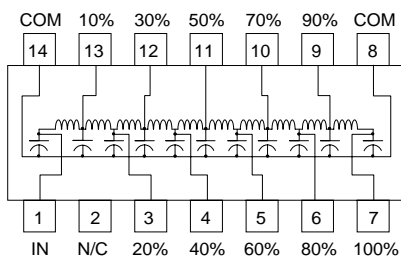
Delay Tolerances		50 Ohm Impedance			75 Ohm Impedance			100 Ohm Impedance			200 Ohm Impedance		
Total (ns)	Tap-to-Tap (ns)	Part Number	Rise Time max. (ns)	DCR max. (Ohms)	Part Number	Rise Time max. (ns)	DCR max. (Ohms)	Part Number	Rise Time max. (ns)	DCR max. (Ohms)	Part Number	Rise Time max. (ns)	DCR max. (Ohms)
5 ± 0.50	0.5 ± 0.2	AIZ-55	1.5	0.8	AIZ-57	1.5	0.8	AIZ-51	1.5	0.8	AIZ-52	1.5	0.8
10 ± 1.00	1.0 ± 0.3	AIZ-105	2.0	0.8	AIZ-107	2.0	1.1	AIZ-101	2.0	1.2	AIZ-102	2.0	1.7
15 ± 1.00	1.5 ± 0.5	AIZ-155	3.0	1.0	AIZ-157	3.0	1.3	AIZ-151	3.0	1.4	AIZ-152	3.3	1.9
20 ± 1.00	2.0 ± 0.5	AIZ-205	4.0	1.2	AIZ-207	4.0	1.5	AIZ-201	4.0	1.6	AIZ-202	4.5	2.4
25 ± 1.25	2.5 ± 0.5	AIZ-255	5.0	1.3	AIZ-257	5.0	1.6	AIZ-251	5.0	1.8	AIZ-252	2.6	3.4
30 ± 1.50	3.0 ± 0.6	AIZ-305	6.0	1.4	AIZ-307	6.0	1.9	AIZ-301	6.0	2.0	AIZ-302	7.2	3.7
35 ± 1.75	3.5 ± 1.0	AIZ-355	7.0	1.5	AIZ-357	7.0	2.6	AIZ-351	7.0	2.9	AIZ-352	8.0	4.0
40 ± 2.00	4.0 ± 1.0	AIZ-405	8.0	1.6	AIZ-407	8.0	2.9	AIZ-401	8.0	3.1	AIZ-402	9.1	4.3
50 ± 2.50	5.0 ± 1.0	AIZ-505	10.0	1.8	AIZ-507	10.0	3.2	AIZ-501	10.0	3.5	AIZ-502	11.0	5.6
60 ± 3.00	6.0 ± 1.5	AIZ-605	12.0	2.0	AIZ-607	12.0	3.5	AIZ-601	12.0	3.8	AIZ-602	12.9	6.1
70 ± 3.50	7.0 ± 1.5	AIZ-705	14.0	2.8	AIZ-707	14.0	4.1	AIZ-701	14.0	4.6	AIZ-702	14.8	6.6
75 ± 3.75	7.5 ± 1.5	AIZ-755	15.0	2.9	AIZ-757	15.0	4.5	AIZ-751	15.0	4.8	AIZ-752	15.7	6.8
80 ± 4.00	8.0 ± 1.8	AIZ-805	16.0	3.0	AIZ-807	16.0	4.8	AIZ-801	16.0	5.0	AIZ-802	16.7	7.0
100 ± 5.00	10.0 ± 2.0	AIZ-1005	20.0	3.4	AIZ-1007	20.0	4.9	AIZ-1001	20.0	5.6	AIZ-1002	21.0	8.2
125 ± 6.25	12.5 ± 2.5	AIZ-1255	25.0	3.8	AIZ-1257	25.0	5.6	AIZ-1251	25.0	6.2	AIZ-1252	25.0	9.5
150 ± 7.50	15.0 ± 3.0	AIZ-1505	30.0	4.8	AIZ-1507	30.0	6.3	AIZ-1501	30.0	6.8	AIZ-1502	30.0	9.8
200 ± 10.00	20.0 ± 3.0	AIZ-2005	40.0	5.7	AIZ-2007	40.0	7.3	AIZ-2001	40.0	7.9	AIZ-2002	40.0	9.9

1. Rise Times are measured from 10% to 90% points.
2. Delay Times measured at 50% point of leading edge.
3. Output (100% Tap) terminated to ground through $R_L = Z_0$.

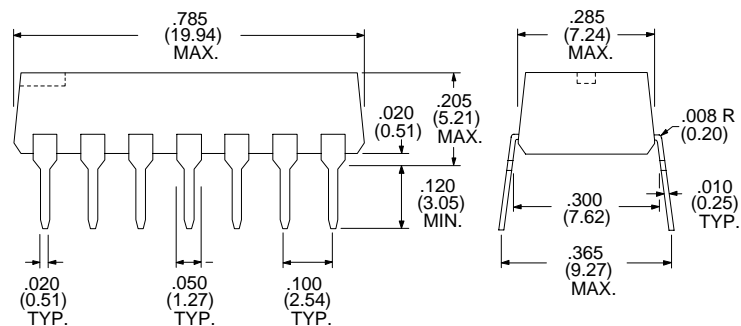
ALTERNATE SCHEMATICS With similar electricals per table , 10 tap passive delays are available in range of schematic styles (Contact factory for others not shown).

AIZ Style Schematic

Most Popular Footprint

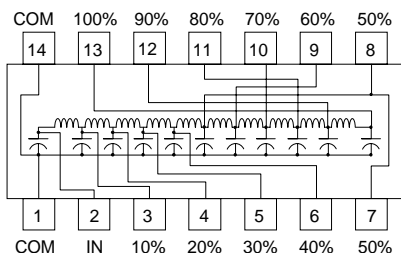


Dimensions in Inches (mm)



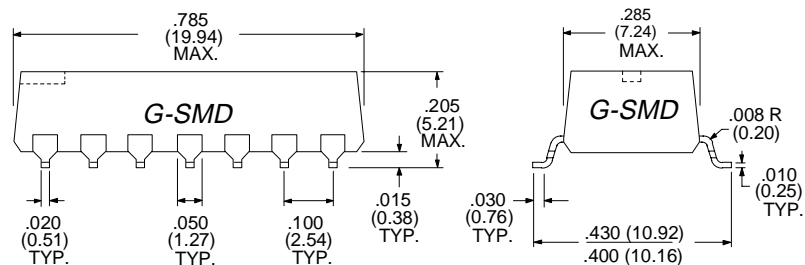
AIU Style Schematic

Per table above, substitute AIU for AIZ in P/N



To Specify G-SMD, Add "G" Suffix to P/N

Examples: AIZ-51G, AIZ-1505G etc.



Specifications subject to change without notice.

For other values & Custom Designs, contact factory.

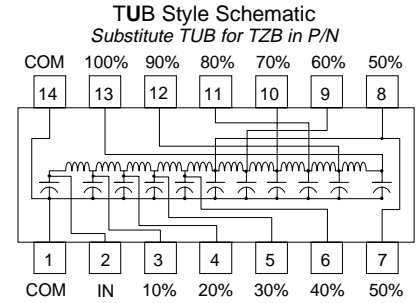
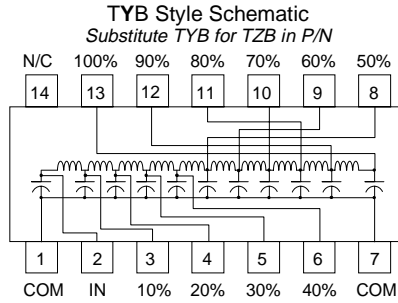
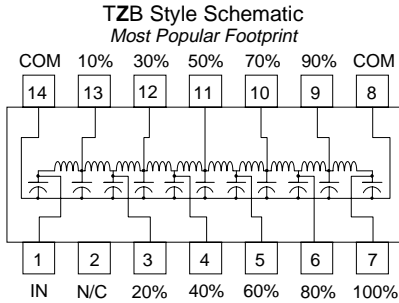
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TZB-TYB-TUB Series 10-Tap High Performance Passive Delays

- Fast Rise Time, Low DCR
- High Bandwidth $\approx 0.35 / t_r$
- Low Distortion LC Network
- 10 Equal Delay Taps
- Standard Impedances: 50 - 75 - 100 - 200 Ω
- Stable Delay vs. Temperature: 100 ppm/ $^{\circ}C$
- Operating Temperature Range -55 $^{\circ}C$ to +125 $^{\circ}C$

Operating Specifications - Passive Delay Lines

- Pulse Overshoot (Pos) 5% to 10%, typical
- Pulse Distortion (S) 3% typical
- Working Voltage 25 VDC maximum
- Dielectric Strength 100VDC minimum
- Insulation Resistance 1,000 M Ω min. @ 100VDC
- Temperature Coefficient 100 ppm/ $^{\circ}C$, typical
- Bandwidth (f_c) 0.35/ t_r approx.
- Operating Temperature Range -55 $^{\circ}$ to +125 $^{\circ}C$
- Storage Temperature Range -65 $^{\circ}$ to +150 $^{\circ}C$



Electrical Specifications at 25 $^{\circ}C$

Delay Tolerances		50 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	75 Ohm Part Number		Rise Time (ns)	DCR max. (Ohms)	100 Ohm Part Number		Rise Time (ns)	DCR max. (Ohms)	200 Ohm Part Number		Rise Time (ns)	DCR max. (Ohms)
Total (ns)	Tap-to-Tap (ns)				Part Number	Part Number			Part Number	Part Number			Part Number	Part Number		
5 \pm 0.5	0.5 \pm 0.2	TZB1-5	2.0	0.7	TZB1-7	2.1	0.8	TZB1-10	2.2	0.8	TZB1-20	2.4	0.9			
10 \pm 0.7	1.0 \pm 0.4	TZB6-5	3.2	0.7	TZB6-7	3.6	0.8	TZB6-10	3.8	0.8	TZB6-20	5.5	1.0			
20 \pm 1.0	2.0 \pm 0.5	TZB12-5	4.0	0.7	TZB12-7	4.4	1.3	TZB12-10	4.6	1.5	TZB12-20	8.5	1.5			
25 \pm 1.25	2.5 \pm 0.5	TZB18-5	4.5	0.9	TZB18-7	5.3	1.5	TZB18-10	5.5	1.7	TZB18-20	9.0	1.8			
30 \pm 1.5	3.0 \pm 0.5	TZB24-5	5.5	1.0	TZB24-7	5.8	1.7	TZB24-10	5.8	2.0	TZB24-20	10.0	2.0			
40 \pm 2.0	4.0 \pm 1.0	TZB30-5	7.0	1.2	TZB30-7	7.5	2.0	TZB30-10	7.5	2.2	TZB30-20	13.0	2.2			
50 \pm 2.5	5.0 \pm 1.0	TZB36-5	8.5	1.3	TZB36-7	8.5	2.1	TZB36-10	8.5	2.3	TZB36-20	15.5	2.4			
60 \pm 3.0	6.0 \pm 1.5	TZB42-5	10.5	1.6	TZB42-7	11.4	2.3	TZB42-10	11.5	2.5	TZB42-20	16.0	2.5			
70 \pm 3.5	7.0 \pm 1.5	TZB48-5	11.0	1.7	TZB48-7	13.0	2.5	TZB48-10	13.0	2.8	TZB48-20	17.0	2.5			
80 \pm 4.0	8.0 \pm 1.8	TZB54-5	12.0	1.9	TZB54-7	15.3	3.8	TZB54-10	15.5	3.0	TZB54-20	19.0	2.5			
90 \pm 4.5	9.0 \pm 2.0	TZB60-5	14.0	2.0	TZB60-7	17.3	3.0	TZB60-10	17.5	3.1	TZB60-20	20.0	2.5			
100 \pm 5.0	10.0 \pm 2.0	TZB66-5	18.0	2.1	TZB66-7	19.5	3.1	TZB66-10	20.0	3.2	TZB66-20	24.0	2.5			
150 \pm 7.50	15.0 \pm 3.0	TZB72-5	24.0	2.2	TZB72-7	26.0	3.3	TZB72-10	26.0	3.5	TZB72-20	35.0	3.6			
200 \pm 10.0	20.0 \pm 3.0	TZB78-5	34.0	2.4	TZB78-7	38.0	3.4	TZB78-10	39.0	3.5	TZB78-20	44.0	4.8			
250 \pm 12.5	25.0 \pm 3.0	TZB84-5	41.0	2.4	TZB84-7	45.0	3.5	TZB84-10	46.0	4.0	TZB84-20	56.0	5.2			
300 \pm 15.0	30.0 \pm 3.0	TZB90-5	48.0	2.5	TZB90-7	53.0	3.5	TZB90-10	54.0	4.2	TZB90-20	68.0	5.8			
400 \pm 20.0	40.0 \pm 5.0	TZB94-5	65.0	2.8	TZB94-7	66.0	3.6	TZB94-10	67.0	4.5	---	---	---			
500 \pm 25.0	50.0 \pm 5.0	TZB98-5	75.0	3.3	TZB98-7	84.0	3.7	TZB98-10	86.0	5.0	---	---	---			

1. Rise Times are measured from 10% to 90% points.
2. Delay Times measured at 50% points of leading edge.
3. Output (100% Tap) terminated to ground through $R_L = Z_0$.

P/N Description

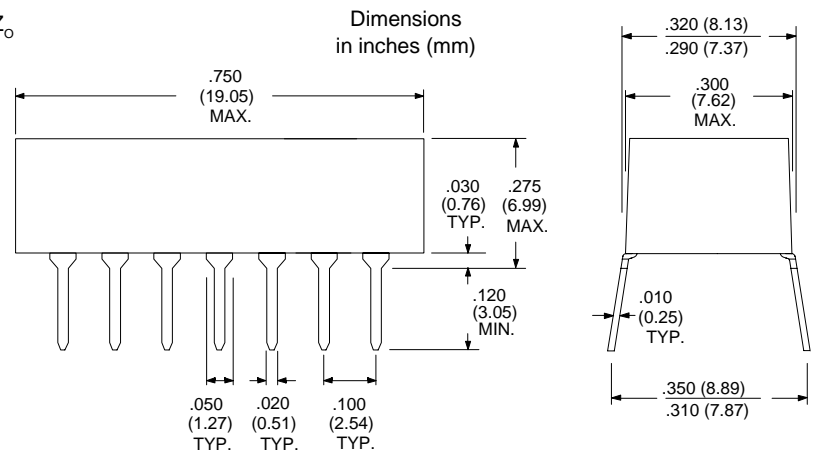
Passive 10 Tap Thru-hole 14-pin Delay Module Series

Delay Coding Number Per Table above

Impedance Specifier:
 50 Ohms = 5
 75 Ohms = 7
 100 Ohms = 10
 200 Ohms = 20

Part Number Examples:

- TZB6-10 = 10 ns, 1 ns / tap, 100 Ω , 14-pin
- TZB18-7 = 25 ns, 2.5 ns / tap, 75 Ω , 14-pin
- TZB98-5 = 500 ns, 50 ns / tap, 50 Ω , 14-pin



Specifications subject to change without notice.

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SIP4 & SIP5 Series High Performance Passive Delay Modules

- Fast Rise Time, Low DCR
- High Bandwidth $\approx 0.35 / t_r$
- Low Distortion LC Network
- 5 or 10 Equal Delay Taps
- Standard Impedances: 50 - 75 - 100 - 200 Ω
- Stable Delay vs. Temperature: 100 ppm/ $^{\circ}C$
- Operating Temperature Range -55 $^{\circ}C$ to +125 $^{\circ}C$

Operating Specifications - Passive Delay Lines

Pulse Overshoot (Pos)	5% to 10%, typical
Pulse Distortion (S)	3% typical
Working Voltage	25 VDC maximum
Dielectric Strength	100VDC minimum
Insulation Resistance	1,000 M Ω min. @ 100VDC
Temperature Coefficient	100 ppm/ $^{\circ}C$, typical
Bandwidth (f_c)	0.35/ t_r approx.
Operating Temperature Range	-55 $^{\circ}$ to +125 $^{\circ}C$
Storage Temperature Range	-65 $^{\circ}$ to +150 $^{\circ}C$

Electrical Specifications at 25 $^{\circ}C$

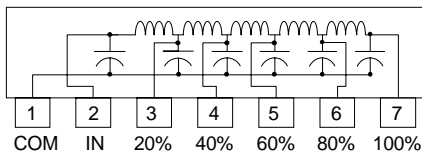
Delay Tolerances		50 Ohm 5-Tap P/N	Rise Time (ns)	DCR max. (Ohms)	75 Ohm 5-Tap P/N		Rise Time (ns)	DCR max. (Ohms)	100 Ohm 5-Tap P/N		Rise Time (ns)	DCR max. (Ohms)	200 Ohm 5-Tap P/N		Rise Time (ns)	DCR max. (Ohms)
Total (ns)	Tap-to-Tap (ns)															
5 \pm 0.5	1.0 \pm 0.4	SIP4-55	2.0	0.7	SIP4-57	2.7	0.8	SIP4-51	3.0	0.8	SIP4-52	3.0	0.9			
10 \pm 1.0	2.0 \pm 0.5	SIP4-105	4.0	0.7	SIP4-107	4.4	1.3	SIP4-101	4.6	1.3	SIP4-102	6.3	1.5			
15 \pm 1.0	3.0 \pm 0.6	SIP4-155	5.5	1.0	SIP4-157	5.8	1.6	SIP4-151	5.8	1.6	SIP4-152	7.7	2.0			
20 \pm 1.0	4.0 \pm 0.8	SIP4-205	6.4	1.2	SIP4-207	7.3	1.7	SIP4-201	7.5	1.7	SIP4-202	9.8	2.2			
25 \pm 1.25	5.0 \pm 1.0	SIP4-255	8.0	1.3	SIP4-257	8.0	1.9	SIP4-251	8.0	1.9	SIP4-252	15.5	2.4			
30 \pm 1.5	6.0 \pm 1.5	SIP4-305	9.0	1.6	SIP4-307	8.5	2.2	SIP4-301	8.5	2.2	SIP4-302	16.0	2.8			
40 \pm 2.0	8.0 \pm 2.0	SIP4-405	11.0	1.9	SIP4-407	15.5	2.7	SIP4-401	15.5	2.8	SIP4-402	17.0	3.4			
50 \pm 2.5	10.0 \pm 2.0	SIP4-505	14.0	2.1	SIP4-507	17.8	2.9	SIP4-501	18.0	3.1	SIP4-502	19.0	4.0			
75 \pm 3.75	15.0 \pm 3.5	SIP4-755	23.0	2.2	SIP4-757	25.7	3.3	SIP4-751	26.0	3.4	-	-	-			
100 \pm 5.0	20.0 \pm 4.0	SIP4-1005	33.0	2.4	SIP4-1007	34.0	3.6	SIP4-1001	34.0	3.7	-	-	-			

Delay Tolerances		50 Ohm 10-Tap P/N	Rise Time (ns)	DCR max. (Ohms)	75 Ohm 10-Tap P/N		Rise Time (ns)	DCR max. (Ohms)	100 Ohm 10-Tap P/N		Rise Time (ns)	DCR max. (Ohms)	200 Ohm 10-Tap P/N		Rise Time (ns)	DCR max. (Ohms)
Total (ns)	Tap-to-Tap (ns)															
5 \pm 0.5	0.5 \pm 0.2	SIP5-55	2.0	0.7	SIP5-57	2.1	0.8	SIP5-51	2.2	0.8	SIP5-52	2.4	0.9			
10 \pm 0.7	1.0 \pm 0.4	SIP5-105	3.2	0.7	SIP5-107	3.6	0.8	SIP5-101	3.8	0.8	SIP5-102	5.5	1.0			
15 \pm 1.0	1.5 \pm 0.5	SIP5-155	3.4	0.8	SIP5-157	4.1	1.2	SIP5-151	4.1	1.3	SIP5-152	6.3	1.5			
20 \pm 1.0	2.0 \pm 0.5	SIP5-205	4.0	0.8	SIP5-207	4.4	1.3	SIP5-201	4.6	1.5	SIP5-202	8.5	1.5			
25 \pm 1.25	2.5 \pm 0.5	SIP5-255	4.5	0.9	SIP5-257	5.3	1.5	SIP5-251	5.5	1.7	SIP5-252	9.0	2.2			
30 \pm 1.5	3.0 \pm 0.6	SIP5-305	5.5	1.0	SIP5-307	5.8	1.7	SIP5-301	5.8	2.0	SIP5-302	10.0	2.4			
40 \pm 2.0	4.0 \pm 1.0	SIP5-405	7.0	1.2	SIP5-407	7.5	2.0	SIP5-401	7.5	2.2	SIP5-402	13.4	3.0			
50 \pm 2.5	5.0 \pm 1.0	SIP5-505	8.5	1.3	SIP5-507	8.5	2.1	SIP5-501	8.5	2.3	SIP5-502	15.5	3.3			
60 \pm 3.0	6.0 \pm 1.5	SIP5-605	10.5	1.6	SIP5-607	11.4	2.3	SIP5-601	11.5	2.5	SIP5-602	16.2	3.6			
75 \pm 3.75	7.5 \pm 1.5	SIP5-755	11.6	1.9	SIP5-757	15.0	2.8	SIP5-751	15.3	3.0	SIP5-752	19.1	3.8			
100 \pm 5.0	10.0 \pm 2.0	SIP5-1005	18.0	2.1	SIP5-1007	19.5	3.1	SIP5-1001	20.0	3.2	SIP5-1002	24.0	4.4			

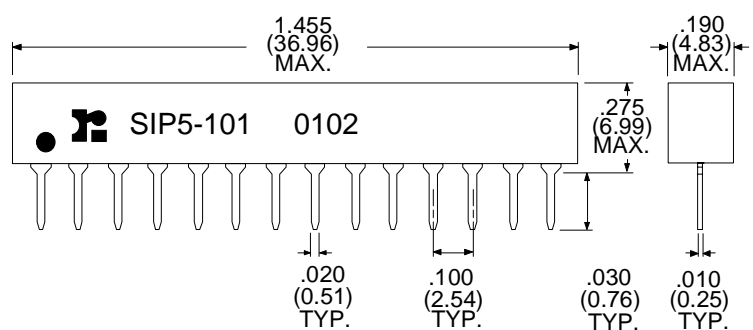
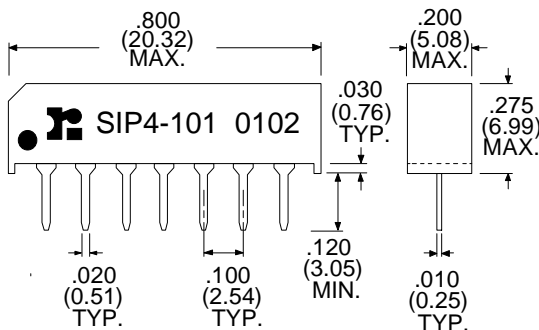
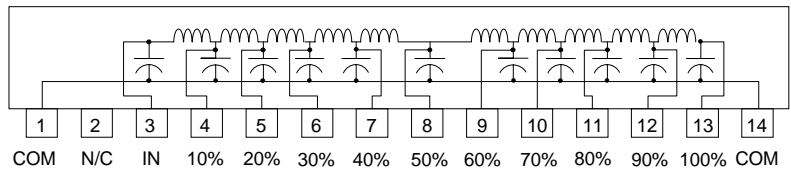
1. Rise Times are measured from 10% to 90% points.
2. Delay Times measured at 50% points of leading edge.
3. Output (100% Tap) terminated to ground through $R_L = Z_0$.

**Low-profile DIP/SMD versions
refer to AIZ & AMZ Series !!!**

5-Tap SIP4 Style Schematic



10-Tap SIP5 Style Schematic



Specifications subject to change without notice.

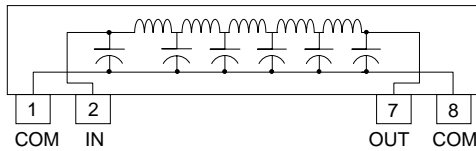
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SIP8 Series High Performance Passive Delays

- Fast Rise Time, Low DCR
- High Bandwidth $\approx 0.35/t_r$
- Low Distortion LC Network
- Single Precise Delay Output
- Standard Impedances: 50 - 75 - 100 - 200 Ω
- Stable Delay vs. Temperature: 100 ppm/°C
- Operating Temperature Range -55°C to +125°C

SIP8 Style Schematic



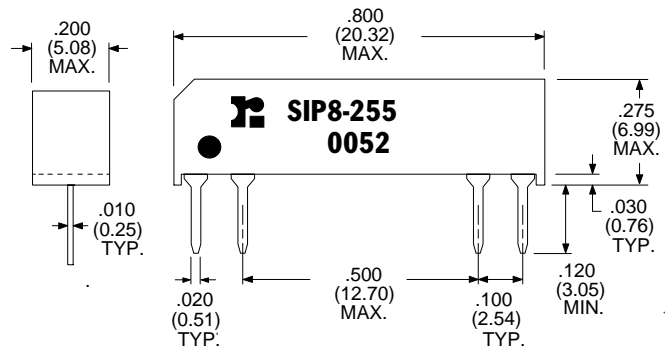
Operating Specifications - Passive Delay Lines

Pulse Overshoot (Pos)	5% to 10%, typical
Pulse Distortion (S)	3% typical
Working Voltage	25 VDC maximum
Dielectric Strength	100VDC minimum
Insulation Resistance	1,000 M Ω min. @ 100VDC
Temperature Coefficient	100 ppm/°C, typical
Bandwidth (f_c)	$0.35/t_r$ approx.
Operating Temperature Range	-55° to +125°C
Storage Temperature Range	-65° to +150°C

Electrical Specifications @ 25°C (1, 2, 3)

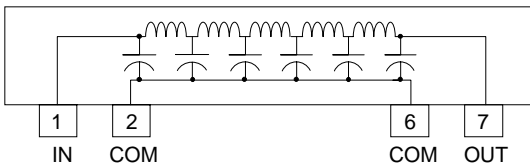
Delay (ns)	Rise Time max. (ns)	DCR max. (Ohms)	50 Ohm Impedance Part Number	75 Ohm Impedance Part Number	93 Ohm Impedance Part Number	100 Ohm Impedance Part Number
1.0 ± .20	0.8	0.8	SIP8-15	SIP8-17	SIP8-19	SIP8-11
1.5 ± .30	0.9	1.1	SIP8-1.55	SIP8-1.57	SIP8-1.59	SIP8-1.51
2.0 ± .30	1.1	1.2	SIP8-25	SIP8-27	SIP8-29	SIP8-21
2.5 ± .30	1.1	1.3	SIP8-2.55	SIP8-2.57	SIP8-2.59	SIP8-2.51
3.0 ± .30	1.3	1.4	SIP8-35	SIP8-37	SIP8-39	SIP8-31
4.0 ± .30	1.6	1.5	SIP8-45	SIP8-47	SIP8-49	SIP8-41
5.0 ± .30	1.8	1.5	SIP8-55	SIP8-57	SIP8-59	SIP8-51
10 ± .50	2.5	1.7	SIP8-105	SIP8-107	SIP8-109	SIP8-101
15 ± .70	3.7	2.1	SIP8-155	SIP8-157	SIP8-159	SIP8-151
20 ± 1.0	4.6	2.4	SIP8-205	SIP8-207	SIP8-209	SIP8-201
25 ± 1.2	5.4	3.1	SIP8-255	SIP8-257	SIP8-259	SIP8-251
30 ± 0.5	6.5	4.5	SIP8-305	SIP8-307	SIP8-309	SIP8-301
50 ± 2.0	10.0	4.5	SIP8-505	SIP8-507	SIP8-509	SIP8-501
100 ± 5.0	20.0	6.2	SIP8-1005	SIP8-1007	SIP8-1009	SIP8-1001
200 ± 10	44.0	7.6	SIP8-2005	SIP8-2007	SIP8-2009	SIP8-2001

Dimensions inches (mm)

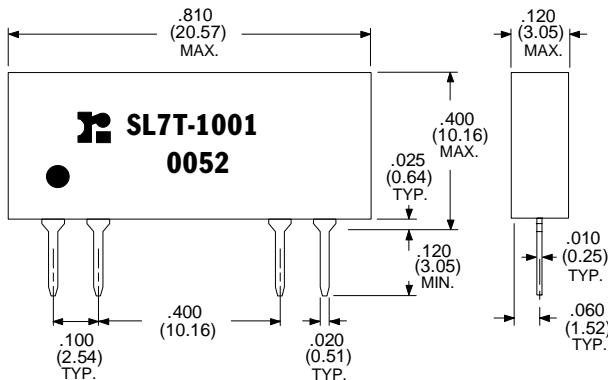


SL7T Series Thin SIP Passive Single Output High Performance Delays

SL7T Schematic Diagram



Dimensions inches (mm)



Electrical Specifications at 25°C 1, 2, 3

Delay (ns)	Rise Time 10%-90% max. (ns)	DCR max. (Ohms)	50 Ohm Impedance Part Number	75 Ohm Impedance Part Number	100 Ohm Impedance Part Number
1.0 ± .20	0.8	0.8	SL7T-15	SL7T-17	SL7T-11
1.5 ± .25	0.9	1.1	SL7T-1P55	SL7T-1P57	SL7T-1P51
2.0 ± .30	1.1	1.2	SL7T-25	SL7T-27	SL7T-21
2.5 ± .30	1.1	1.3	SL7T-2P55	SL7T-2P57	SL7T-2P51
3.0 ± .30	1.3	1.4	SL7T-35	SL7T-37	SL7T-31
3.5 ± .50	1.5	1.5	SL7T-3P55	SL7T-3P57	SL7T-3P51
4.0 ± .50	1.6	1.5	SL7T-45	SL7T-47	SL7T-41
5.0 ± .50	1.8	1.5	SL7T-55	SL7T-57	SL7T-51
6.0 ± .60	1.9	1.5	SL7T-65	SL7T-67	SL7T-61
7.0 ± .70	2.1	1.5	SL7T-75	SL7T-77	SL7T-71
7.5 ± .75	2.2	1.6	SL7T-7P55	SL7T-7P57	SL7T-7P51
8.0 ± .75	2.2	1.6	SL7T-85	SL7T-87	SL7T-81
10.0 ± .75	2.5	1.7	SL7T-105	SL7T-107	SL7T-101
12.5 ± .75	2.5	1.9	SL7T-12P55	SL7T-12P57	SL7T-12P51
15.0 ± .75	2.7	2.1	SL7T-155	SL7T-157	SL7T-151
20.0 ± 1.0	4.6	2.4	SL7T-205	SL7T-207	SL7T-201
25.0 ± 1.25	5.4	2.9	SL7T-255	SL7T-257	SL7T-251
30.0 ± 1.5	6.5	3.0	SL7T-305	SL7T-307	SL7T-301
40.0 ± 2.0	8.5	3.3	SL7T-405	SL7T-407	SL7T-401
50.0 ± 2.5	10.0	3.5	SL7T-505	SL7T-507	SL7T-501
75.0 ± 3.75	15.0	4.8	SL7T-755	SL7T-757	SL7T-751
100 ± 5.0	20.0	5.6	SL7T-1005	SL7T-1007	SL7T-1001

1. Rise Times are measured from 10% to 90% points.
2. Delay Times measured at 50% points of leading edge.
3. Output terminated to ground through $R_L = Z_0$

Specifications subject to change without notice.

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SIL2 Series Mini-SIP Passive Delay Modules

- Fast Rise Time, Low DCR
- High Bandwidth $\approx 0.35 / t_r$
- Low Distortion LC Network
- Tight Delay Tolerance
- Standard Impedances: 50 to 200 Ω
- Stable Delay vs. Temperature: 100 ppm/°C
- Operating Temperature Range -55°C to +125°C

Operating Specifications - Passive Delay Lines

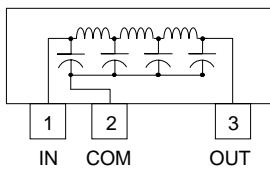
Pulse Overshoot (Pos)	5% to 10%, typical
Pulse Distortion (S)	3% typical
Working Voltage	25 VDC maximum
Dielectric Strength	100VDC minimum
Insulation Resistance	1,000 M Ω min. @ 100VDC
Temperature Coefficient	100 ppm/°C, typical
Bandwidth (f_c)	0.35/ t_r approx.
Operating Temperature Range	-55° to +125°C
Storage Temperature Range	-65° to +150°C

Electrical Specifications at 25°C

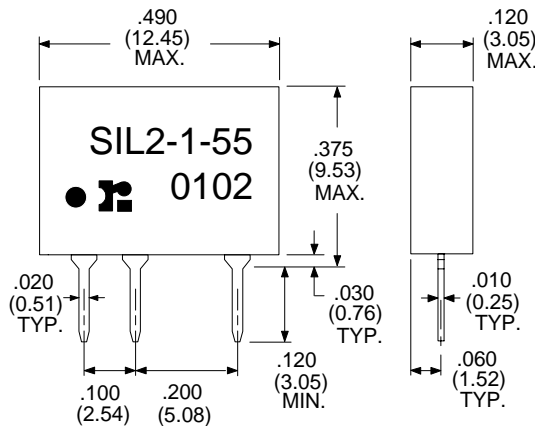
Delay (ns)	Rise Time max. (ns)	DCR max. (Ohms)	50 Ohm Impedance Part Number	55 Ohm Impedance Part Number	60 Ohm Impedance Part Number	75 Ohm Impedance Part Number	93 Ohm Impedance Part Number	100 Ohm Impedance Part Number	200 Ohm Impedance Part Number
0.0	—	.10	SIL2-0	SIL2-0	SIL2-0	SIL2-0	SIL2-0	SIL2-0	SIL2-0
1.0 \pm .20	1.6	.20	SIL2-1-50	SIL2-1-55	SIL2-1-60	SIL2-1-75	SIL2-1-93	SIL2-1-10	SIL2-1-20
1.5 \pm .20	1.6	.30	SIL2-1.5-50	SIL2-1.5-55	SIL2-1.5-60	SIL2-1.5-75	SIL2-1.5-93	SIL2-1.5-10	SIL2-1.5-20
2.0 \pm .20	1.6	.40	SIL2-2-50	SIL2-2-55	SIL2-2-60	SIL2-2-75	SIL2-2-93	SIL2-2-10	SIL2-2-20
2.5 \pm .20	1.6	.50	SIL2-2.5-50	SIL2-2.5-55	SIL2-2.5-60	SIL2-2.5-75	SIL2-2.5-93	SIL2-2.5-10	SIL2-2.5-20
3.0 \pm .20	1.7	.60	SIL2-3-50	SIL2-3-55	SIL2-3-60	SIL2-3-75	SIL2-3-93	SIL2-3-10	SIL2-3-20
4.0 \pm .20	1.7	.70	SIL2-4-50	SIL2-4-55	SIL2-4-60	SIL2-4-75	SIL2-4-93	SIL2-4-10	SIL2-4-20
5.0 \pm .25	1.8	.80	SIL2-5-50	SIL2-5-55	SIL2-5-60	SIL2-5-75	SIL2-5-93	SIL2-5-10	SIL2-5-20
6.0 \pm .30	2.0	.85	SIL2-6-50	SIL2-6-55	SIL2-6-60	SIL2-6-75	SIL2-6-93	SIL2-6-10	SIL2-6-20
7.0 \pm .30	2.3	.90	SIL2-7-50	SIL2-7-55	SIL2-7-60	SIL2-7-75	SIL2-7-93	SIL2-7-10	SIL2-7-20
8.0 \pm .30	2.7	.95	SIL2-8-50	SIL2-8-55	SIL2-8-60	SIL2-8-75	SIL2-8-93	SIL2-8-10	SIL2-8-20
9.0 \pm .30	2.9	1.10	SIL2-9-50	SIL2-9-55	SIL2-9-60	SIL2-9-75	SIL2-9-93	SIL2-9-10	SIL2-9-20
10 \pm .30	3.3	1.20	SIL2-10-50	SIL2-10-55	SIL2-10-60	SIL2-10-75	SIL2-10-93	SIL2-10-10	SIL2-10-20
11 \pm .40	3.8	1.40	SIL2-11-50	SIL2-11-55	SIL2-11-60	SIL2-11-75	SIL2-11-93	SIL2-11-10	SIL2-11-20
12 \pm .50	4.1	1.50	SIL2-12-50	SIL2-12-55	SIL2-12-60	SIL2-12-75	SIL2-12-93	SIL2-12-10	SIL2-12-20
13 \pm .60	4.6	1.60	SIL2-13-50	SIL2-13-55	SIL2-13-60	SIL2-13-75	SIL2-13-93	SIL2-13-10	SIL2-13-20
14 \pm .70	4.9	1.60	SIL2-14-50	SIL2-14-55	SIL2-14-60	SIL2-14-75	SIL2-14-93	SIL2-14-10	SIL2-14-20
15 \pm .70	5.3	1.70	SIL2-15-50	SIL2-15-55	SIL2-15-60	SIL2-15-75	SIL2-15-93	SIL2-15-10	SIL2-15-20
16 \pm .80	5.6	1.70	SIL2-16-50	SIL2-16-55	SIL2-16-60	SIL2-16-75	SIL2-16-93	SIL2-16-10	SIL2-16-20
20 \pm 1.0	7.0	2.00	SIL2-20-50	SIL2-20-55	SIL2-20-60	SIL2-20-75	SIL2-20-93	SIL2-20-10	SIL2-20-20

1. Rise Times are measured from 20% to 80% points.
2. Delay Times measured at 50% points of leading edge.
3. Output terminated to ground through $R_L = Z_0$

SIL2 Single Output Schematic



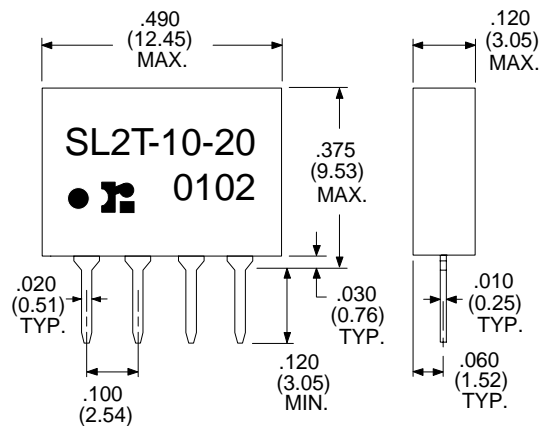
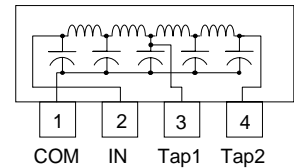
Dimensions in inches (mm)



"SL2T" Part Number Examples:

- SL2T2-50
2 ns (1ns Tap) 50 Ω
- SL2T1.5-55
2.5 ns (1.25ns Tap) 55 Ω
- SL2T12-10
12 ns (6ns Tap) 100 Ω

SL2T 2-tap Schematic



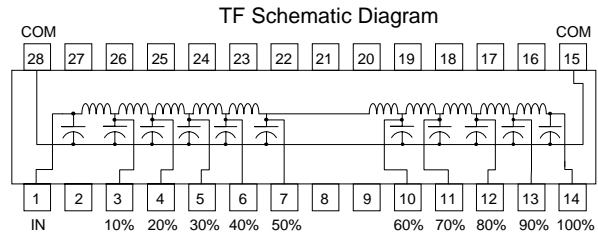
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TF Series High Performance 20 Section 10-Tap Delay Lines

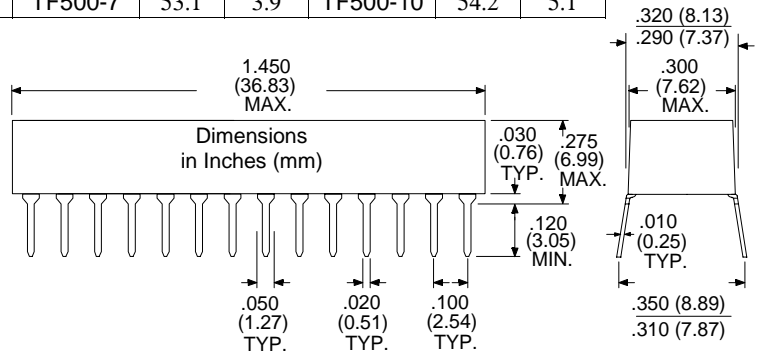
- Fast Rise Time ($t_d/t_r \approx 10$)
- High Bandwidth $\approx 0.35/t_r$
- Low Distortion LC Network
- 10 Equal Delay Taps
- Standard Impedances: 50 - 75 - 100 Ω
- Stable Delay vs. Temperature: 100 ppm/ $^{\circ}\text{C}$
- Operating Temperature Range -55 $^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$



Electrical Specifications at 25 $^{\circ}\text{C}$ 1, 2, 3

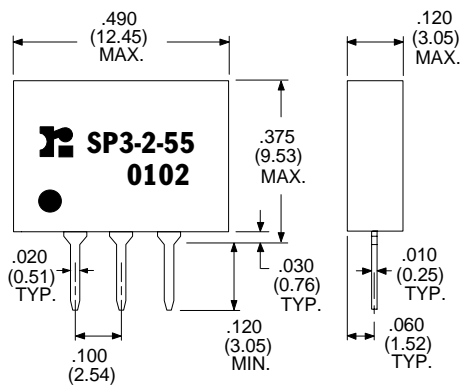
Delay Tolerances		50 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	75 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	100 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)
Total (ns)	Tap-to-Tap (ns)									
50 \pm 2.5	5.0 \pm 1.0	TF50-5	6.2	1.9	TF50-7	6.2	2.0	TF50-10	6.4	2.2
75 \pm 3.7	7.5 \pm 2.0	TF75-5	9.2	2.1	TF75-7	9.2	2.2	TF75-10	9.4	2.3
80 \pm 4.0	8.0 \pm 2.0	TF80-5	9.5	2.2	TF80-7	9.6	2.3	TF80-10	9.9	2.4
100 \pm 5.0	10.0 \pm 2.0	TF100-5	11.2	2.3	TF100-7	11.7	2.5	TF100-10	12.5	2.7
120 \pm 6.0	12.0 \pm 2.0	TF120-5	13.4	2.3	TF120-7	13.7	2.7	TF120-10	13.8	3.1
150 \pm 15.0	15.0 \pm 2.5	TF150-5	15.7	2.4	TF150-7	16.1	3.1	TF150-10	16.4	3.5
200 \pm 10.0	20.0 \pm 3.0	TF200-5	21.3	2.5	TF200-7	21.5	3.3	TF200-10	21.6	3.8
250 \pm 12.5	25.0 \pm 3.0	TF250-5	27.2	2.6	TF250-7	27.3	3.5	TF250-10	27.5	4.3
300 \pm 15.0	30.0 \pm 3.5	TF300-5	31.1	2.7	TF300-7	31.4	3.6	TF300-10	32.3	4.6
400 \pm 20.0	40.0 \pm 4.0	TF400-5	41.0	2.8	TF400-7	41.3	3.7	TF400-10	41.7	4.8
500 \pm 25.0	50.0 \pm 5.0	TF500-5	50.8	2.9	TF500-7	53.1	3.9	TF500-10	54.2	5.1

1. Rise Times are measured from 10% to 90% points.
2. Delay Times measured at 50% points of leading edge.
3. Output (100% Tap) terminated through Z_0 to ground.

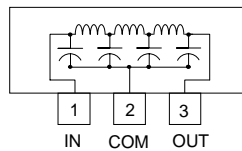


SP3 Series 3-Pin Mini-SIP Passive Delays

Refer to SIL2 Series



SP3 Style Schematic



Part Number Examples:
 SP3-2-50 = 2 ns 50 Ω
 SP3-2.5-93 = 2.5 ns 93 Ω
 SP3-5-10 = 5 ns 100 Ω
 SP3-10-20 = 10 ns 200 Ω

Electrical Specifications at 25 $^{\circ}\text{C}$

Delay (ns)	Rise Time 20% - 80% max. (ns)	DCR max. (Ohms)	Part Number Zo: XX= 50, 55, 75, 93, 10 or 20
1.0 \pm .20	1.6	.20	SP3-1 - XX
1.5 \pm .20	1.6	.30	SP3-1.5 - XX
2.0 \pm .20	1.6	.40	SP3-2 - XX
2.5 \pm .20	1.6	.50	SP3-2.5 - XX
3.0 \pm .20	1.7	.60	SP3-3 - XX
3.5 \pm .20	1.7	.60	SP3-3.5 - XX
4.0 \pm .20	1.7	.70	SP3-4 - XX
4.5 \pm .20	1.7	.70	SP3-4.5 - XX
5.0 \pm .25	1.8	.80	SP3-5 - XX
6.0 \pm .30	2.0	.85	SP3-6 - XX
7.0 \pm .30	2.2	.90	SP3-7 - XX
7.5 \pm .30	2.4	.95	SP3-7.5 - XX
8.0 \pm .30	2.4	.95	SP3-8 - XX
10 \pm .30	2.8	1.20	SP3-10 - XX

1. Rise Times are measured from 20% to 80% points.
2. Delay Times measured at 50% points of leading edge.
3. Output (100% Tap) terminated through Z_0 to ground.

Specifications subject to change without notice.

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SP24A Series 20-Tap High Performance Passive Delay Modules

- Fast Rise Time, Low DCR
- High Bandwidth $\approx 0.35/t_r$
- Low Distortion LC Network
- 20 Equal Delay Taps
- Standard Impedances: 50 - 75 - 100 - 200 Ω
- Stable Delay vs. Temperature: 100 ppm/ $^{\circ}\text{C}$
- Operating Temperature Range -55 $^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$

Operating Specifications - Passive Delay Lines

Pulse Overshoot (Pos)	5% to 10%, typical
Pulse Distortion (S)	3% typical
Working Voltage	25 VDC maximum
Dielectric Strength	100VDC minimum
Insulation Resistance	1,000 M Ω min. @ 100VDC
Temperature Coefficient	70 ppm/ $^{\circ}\text{C}$, typical
Bandwidth (f_c)	0.35/ t_r approx.
Operating Temperature Range	-55 $^{\circ}$ to +125 $^{\circ}\text{C}$
Storage Temperature Range	-65 $^{\circ}$ to +150 $^{\circ}\text{C}$

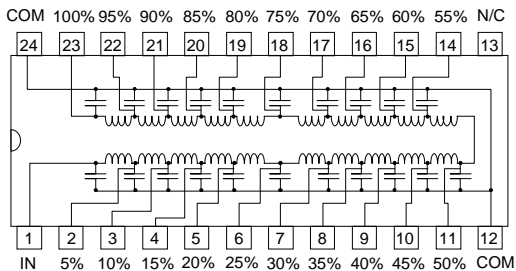
Electrical Specifications ^{1,2,3} at 25 $^{\circ}\text{C}$ Note: For SMD Package Add "G" to end of P/N in Table Below

Total (ns)	Tap-to-Tap (ns)	50 Ohm Part Number	Rise Time max. (ns)	DCR max. (Ohms)	75 Ohm Part Number	Rise Time max. (ns)	DCR max. (Ohms)	100 Ohm Part Number	Rise Time max. (ns)	DCR max. (Ohms)	200 Ohm Part Number	Rise Time max. (ns)	DCR max. (Ohms)
10 \pm 0.50	0.5 \pm 0.2	SP24A-105	2.5	1.0	SP24A-107	2.5	1.0	SP24A-101	2.8	1.3	SP24A-102	3.5	2.5
20 \pm 1.00	1.0 \pm 0.4	SP24A-205	3.7	1.7	SP24A-207	3.7	1.7	SP24A-201	3.7	1.8	SP24A-202	4.0	3.9
25 \pm 1.25	1.25 \pm 0.5	SP24A-255	4.0	1.8	SP24A-257	4.0	1.8	SP24A-251	4.0	2.1	SP24A-252	4.5	4.4
30 \pm 1.50	1.5 \pm 0.5	SP24A-305	4.8	1.9	SP24A-307	4.8	1.9	SP24A-301	4.8	2.3	SP24A-302	5.0	4.8
40 \pm 2.00	2.0 \pm 0.5	SP24A-405	5.5	2.1	SP24A-407	5.5	2.1	SP24A-401	5.5	2.4	SP24A-402	7.5	5.0
50 \pm 2.50	2.5 \pm 0.5	SP24A-505	6.0	2.2	SP24A-507	6.0	2.2	SP24A-501	6.2	2.6	SP24A-502	9.0	5.2
60 \pm 3.00	3.0 \pm 0.6	SP24A-605	7.0	2.4	SP24A-607	7.0	2.4	SP24A-601	7.1	2.7	SP24A-602	10.0	5.3
70 \pm 3.50	3.5 \pm 0.8	SP24A-705	7.9	2.6	SP24A-707	7.9	2.6	SP24A-701	8.1	2.8	SP24A-702	11.0	5.4
75 \pm 3.75	3.75 \pm 0.8	SP24A-755	8.7	2.6	SP24A-757	8.8	2.6	SP24A-751	8.8	2.9	SP24A-752	11.5	5.5
80 \pm 4.00	4.0 \pm 1.0	SP24A-805	9.4	2.8	SP24A-807	9.4	2.8	SP24A-801	9.5	3.0	SP24A-802	12.0	5.7
100 \pm 5.00	5.0 \pm 1.0	SP24A1005	11.8	3.0	SP24A1007	11.9	3.3	SP24A1001	11.9	3.3	SP24A1002	15.0	6.0
150 \pm 7.50	7.5 \pm 2.0	SP24A1505	15.5	3.4	SP24A1507	16.0	3.7	SP24A1501	16.0	3.7	SP24A1502	23.0	7.0
200 \pm 10.0	10.0 \pm 2.0	SP24A2005	20.0	3.6	SP24A2007	18.9	4.1	SP24A2001	18.9	4.1	SP24A2002	31.0	8.1
250 \pm 12.5	12.5 \pm 3.0	SP24A2505	26.0	3.8	SP24A2507	24.5	4.2	SP24A2501	24.5	4.3	SP24A2502	38.0	9.2
300 \pm 15.0	15.0 \pm 3.0	SP24A3005	32.0	4.4	SP24A3007	29.0	4.5	SP24A3001	29.0	4.8	SP24A3002	46.0	9.9
400 \pm 20.0	20.0 \pm 4.0	SP24A4005	38.0	4.5	SP24A4007	38.0	4.7	SP24A4001	38.0	4.9	----	----	----
500 \pm 25.0	25.0 \pm 5.0	SP24A5005	46.0	4.8	SP24A5007	46.0	4.9	SP24A5001	46.0	5.2	----	----	----

1. Rise Times are measured from 10% to 90% points.
2. Delay Times measured at 50% points of leading edge.
3. Output (100% Tap) terminated to ground through $R_L = Z_0$

Dimensions in Inches (mm)

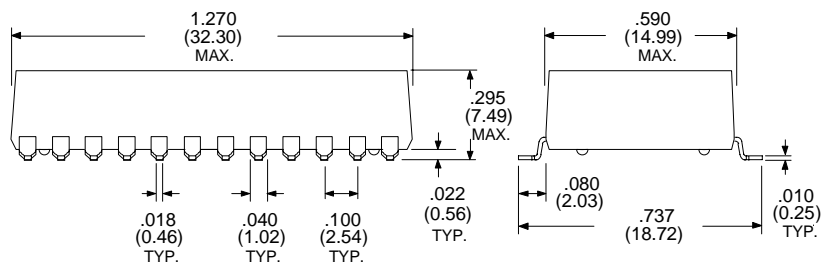
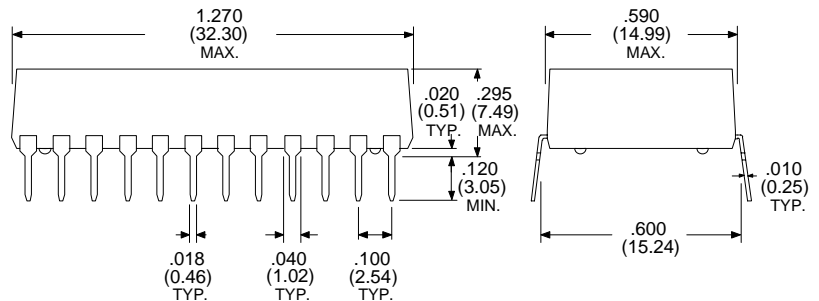
SP24A Style 20-Tap Schematic



Alternate Pinout, Similar 20 Tap Electricals, refer to Series **SP24**

Also, for same 24-Pin package and Single Output refer to Series **SP24L**

Default Thru-hole 24-Pin Package. Example: SP24A-105



Gull wing SMD Package Add suffix "G" to P/N. Example: SP24A-105G

SP24L Series 24-Pin Single Output Passive Delay Modules

Optimized for Fastest Rise times and Lowest DCR in single configuration

- Fast Rise Time, Low DCR
- Better than 10/1 Td/tr typical
- High Bandwidth $\approx 0.35 / t_r$
- Low Distortion LC Network
- Standard Impedances: 50 - 75 - 100 Ω
- Stable Delay vs. Temperature: 100 ppm/ $^{\circ}\text{C}$
- Operating Temperature Range -55 $^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$

Operating Specifications - Passive Delay Lines

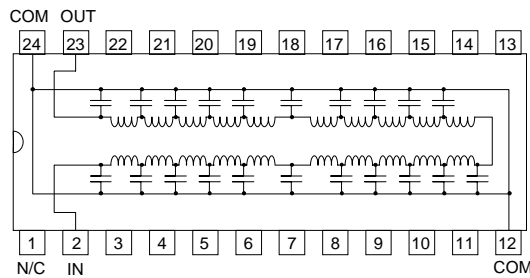
Pulse Overshoot (Pos)	5% to 10%, typical
Pulse Distortion (S)	3% typical
Working Voltage	25 VDC maximum
Dielectric Strength	100VDC minimum
Insulation Resistance	1,000 M Ω min. @ 100VDC
Temperature Coefficient	70 ppm/ $^{\circ}\text{C}$, typical
Bandwidth (f_c)	0.35/ t_r approx.
Operating Temperature Range	-55 $^{\circ}$ to +125 $^{\circ}\text{C}$
Storage Temperature Range	-65 $^{\circ}$ to +150 $^{\circ}\text{C}$

Electrical Specifications ^{1,2,3} at 25 $^{\circ}\text{C}$ Note: For SMD Package Add "G" to end of P/N in Table Below

Delay (ns)	50 Ohm Part Number	Rise Time max. (ns)	DCR max. (Ohms)	75 Ohm Part Number	Rise Time max. (ns)	DCR max. (Ohms)	100 Ohm Part Number	Rise Time max. (ns)	DCR max. (Ohms)
50 \pm 2.50	SP24L-505	5.2	1.5	SP24L-507	5.2	1.8	SP24L-501	5.2	2.0
75 \pm 3.75	SP24L-755	7.1	1.9	SP24L-757	7.1	2.2	SP24L-751	7.3	2.3
100 \pm 5.00	SP24L1005	9.2	2.4	SP24L1007	9.3	2.6	SP24L1001	9.4	2.6
150 \pm 7.50	SP24L1505	13.8	2.5	SP24L1507	14.0	2.7	SP24L1501	14.0	2.7
200 \pm 10.0	SP24L2005	16.5	2.6	SP24L2007	16.5	2.9	SP24L2001	16.5	2.9
250 \pm 12.5	SP24L2505	22.0	2.9	SP24L2507	22.0	3.4	SP24L2501	22.0	3.5
300 \pm 15.0	SP24L3005	22.4	3.1	SP24L3007	22.6	3.7	SP24L3001	22.8	3.9
400 \pm 20.0	SP24L4005	34.0	3.8	SP24L4007	35.0	4.8	SP24L4001	36.0	4.9
500 \pm 25.0	SP24L5005	42.0	4.8	SP24L5007	42.0	5.8	SP24L5001	42.0	6.2
750 \pm 37.5	SP24L7505	69.0	6.4	SP24L7507	69.0	7.1	SP24L7501	69.0	7.2
1000 \pm 50.0	SP24L10005	94.0	7.2	SP24L10007	94.0	8.8	SP24L10001	94.0	9.6
1200 \pm 60.0	SP24L12005	110.0	8.3	SP24L12007	111.0	9.8	SP24L12001	112.0	10.4

1. Rise Times are measured from 10% to 90% points.
2. Delay Times measured at 50% points of leading edge.
3. Output (100% Tap) terminated to ground through $R_L = Z_0$

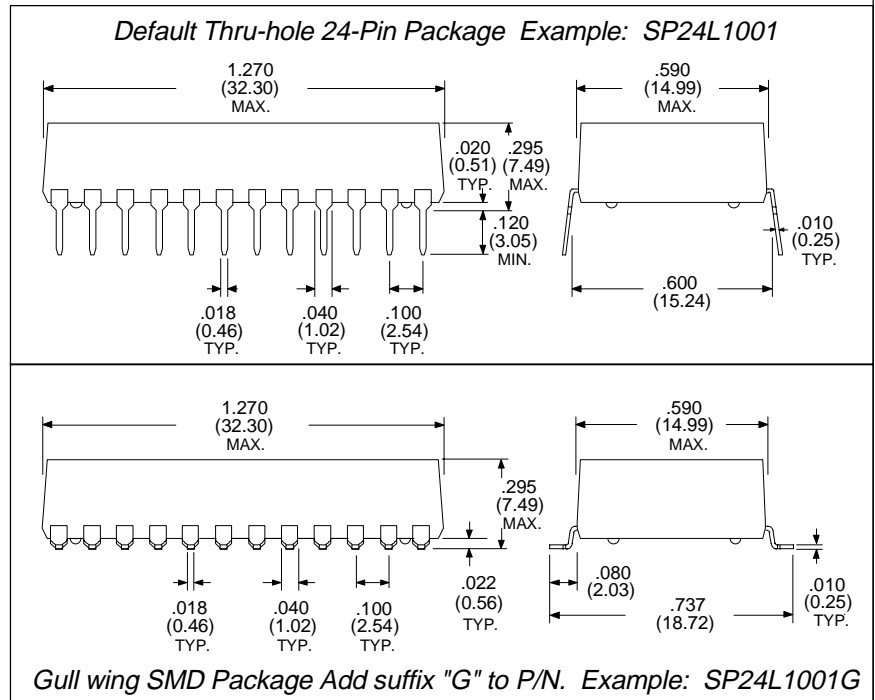
SP24L Style Single Output Schematic



For similar package, alternate schematic style with only one common connection (pin 24 = N/C) at pin 12, refer to Series **SP241**

For 20 Tap versions in the same 24-Pin package, refer to Series **SP24A & SP24A**

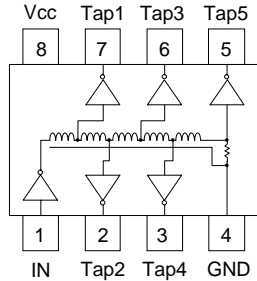
Dimensions in Inches (mm)



FAMDM Series FAST / TTL Buffered 5-Tap Delay Modules

- Low Profile 8-Pin Package
Two Surface Mount Versions
- FAST/TTL Logic Buffered
- 5 Equal Delay Taps
- Operating Temperature
Range 0°C to +70°C
- 14-Pin Versions: FAMDM Series
SIP Versions: FSIDM Series
- Low Voltage CMOS Versions
refer to LVMDM / LVIDM Series

FAMDM 8-Pin Schematic



Electrical Specifications at 25°C

FAST 5 Tap 8-Pin DIP P/N	Tap Delay Tolerances +/- 5% or 2ns (+/- 1ns <13ns)					Tap-to-Tap (ns)
	Tap 1	Tap 2	Tap 3	Tap 4	Total - Tap 5	
FAMDM-7	3.0	4.0	5.0	6.0	7 ± 1.0	** 1 ± 0.5
FAMDM-9	3.0	4.5	6.0	7.5	9 ± 1.0	** 1.5 ± 0.5
FAMDM-11	3.0	5.0	7.0	9.0	11 ± 1.0	** 2 ± 0.7
FAMDM-13	3.0	5.5	8.0	10.5	13 ± 1.5	** 2.5 ± 1.0
FAMDM-15	3.0	6.0	9.0	12.0	15 ± 1.5	3 ± 1.0
FAMDM-20	4.0	8.0	12.0	16.0	20 ± 2.0	4 ± 1.5
FAMDM-25	5.0	10.0	15.0	20.0	25 ± 2.0	5 ± 2.0
FAMDM-30	6.0	12.0	18.0	24.0	30 ± 2.0	6 ± 2.0
FAMDM-35	7.0	14.0	21.0	28.0	35 ± 2.0	7 ± 2.0
FAMDM-40	8.0	16.0	24.0	32.0	40 ± 2.0	8 ± 2.0
FAMDM-50	10.0	20.0	30.0	40.0	50 ± 2.5	10 ± 2.0
FAMDM-60	12.0	24.0	36.0	48.0	60 ± 3.0	12 ± 2.0
FAMDM-75	15.0	30.0	45.0	60.0	75 ± 3.75	15 ± 2.5
FAMDM-100	20.0	40.0	60.0	80.0	100 ± 5.0	20 ± 3.0
FAMDM-125	25.0	50.0	75.0	100.0	125 ± 6.25	25 ± 3.0
FAMDM-150	30.0	60.0	90.0	120.0	150 ± 7.5	30 ± 3.0
FAMDM-200	40.0	80.0	120.0	160.0	200 ± 10.0	40 ± 4.0
FAMDM-250	50.0	100.0	150.0	200.0	250 ± 12.5	50 ± 5.0
FAMDM-350	70.0	140.0	210.0	280.0	350 ± 17.5	70 ± 5.0
FAMDM-500	100.0	200.0	300.0	400.0	500 ± 25.0	100 ± 10.0

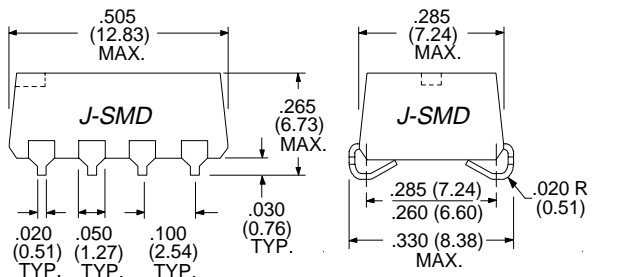
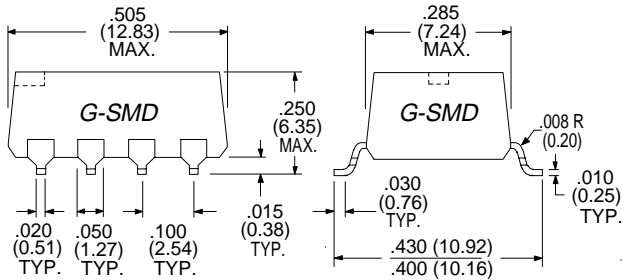
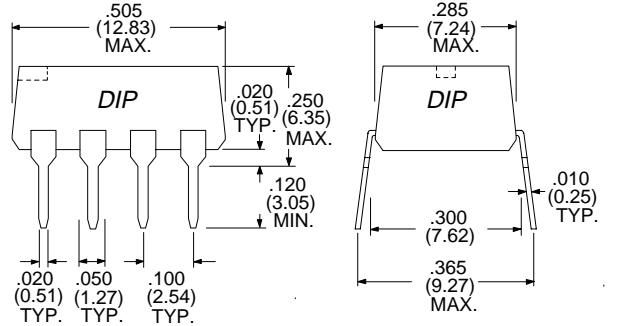
** These part numbers do not have 5 equal taps. Tap-to-Tap Delays reference Tap 1.

TEST CONDITIONS -- FAST / TTL

V_{CC} Supply Voltage 5.00VDC
 Input Pulse Voltage 3.20V
 Input Pulse Rise Time 3.0 ns max.
 Input Pulse Width / Period 1000 / 2000 ns

1. Measurements made at 25°C
2. Delay Times measured at 1.50V level of leading edge.
3. Rise Times measured from 0.75V to 2.40V.
4. 10pf probe and fixture load on output under test.

Dimensions in Inches (mm)



OPERATING SPECIFICATIONS

V_{CC} Supply Voltage 5.00 ± 0.25 VDC
 I_{CC} Supply Current 48 mA Maximum
 Logic "1" Input: V_{IH} 2.00 V min., 5.50 V max.
 I_{IH} 20 µA max. @ 2.70V
 Logic "0" Input: V_{IL} 0.80 V max.
 I_{IL} -0.6 mA mA
 V_{OH} Logic "1" Voltage Out 2.40 V min.
 V_{OL} Logic "0" Voltage Out 0.50 V max.
 P_{WI} Input Pulse Width 40% of Delay min.
 Operating Temperature Range 0° to 70°C
 Storage Temperature Range -65° to +150°C

P/N Description

FAMDM - XXX X

Buffered 5 Tap Delay

Molded Package Series:

8-pin DIP: FAMDM

Total Delay in nanoseconds (ns)

Lead Style: Blank = Thru-hole
 G = "Gull Wing" SMD
 J = "J" Bend SMD

Examples: FAMDM-25G = 25ns (5ns per tap)
 74F, 8-Pin G-SMD

FAMDM-100 = 100ns (20ns per tap)
 74F, 8-Pin DIP

Specifications subject to change without notice.

For other values & Custom Designs, contact factory.

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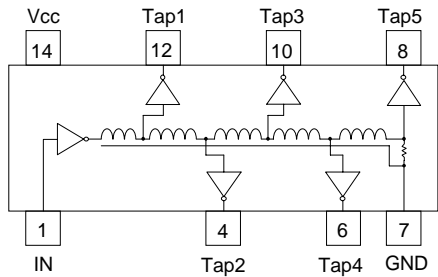
sales@rhombus-ind.com

TEL: (714) 898-0960

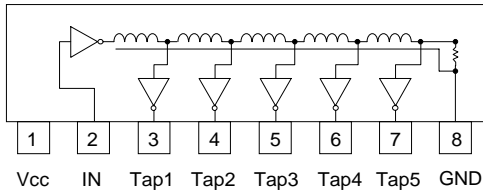
FAX: (714) 896-0971

FAIDM / FSIDM Series FAST / TTL Buffered 5-Tap Delay Modules

FAIDM 14-Pin Schematic



FSIDM 8-Pin SIP Schematic



P/N Description

Logic 5 Tap Delay
Molded Package Series:
14-pin DIP: FAIDM
8-pin SIP: FSIDM
Total Delay in nanoseconds (ns)
Lead Style: Blank = Thru-hole
G = "Gull Wing" SMD (FAIDM Only)

FXIDM - XXX X

Examples: FAIDM-25G = 25ns (5ns per tap)
74F, 14-Pin G-SMD
FAIDM-100 = 100ns (20ns per tap)
74F, 14-Pin DIP
FSIDM-50 = 50ns (10ns per tap)
74F, 8-Pin SIP

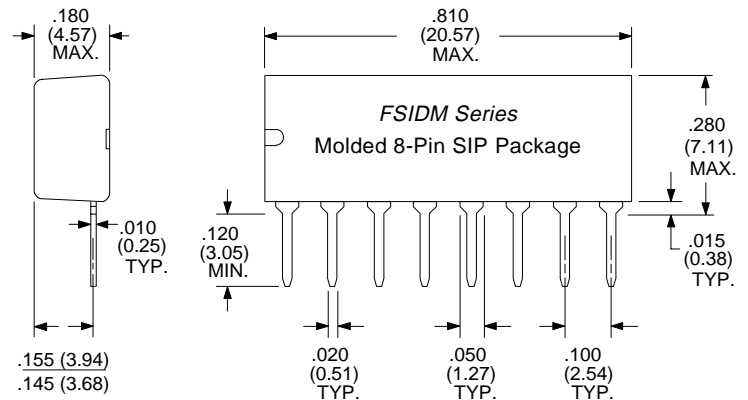
OPERATING SPECIFICATIONS

V_{CC} Supply Voltage 5.00 ± 0.25 VDC
 I_{CC} Supply Current 48 mA Maximum
Logic "1" Input: V_{IH} 2.00 V min., 5.50 V max.
 I_{IH} 20 μ A max. @ 2.70V
Logic "0" Input: V_{IL} 0.80 V max.
 I_{IL} -0.6 mA mA
 V_{OH} Logic "1" Voltage Out 2.40 V min.
 V_{OL} Logic "0" Voltage Out 0.50 V max.
 P_{WI} Input Pulse Width 40% of Delay min.
Operating Temperature Range 0° to 70°C
Storage Temperature Range -65° to +150°C

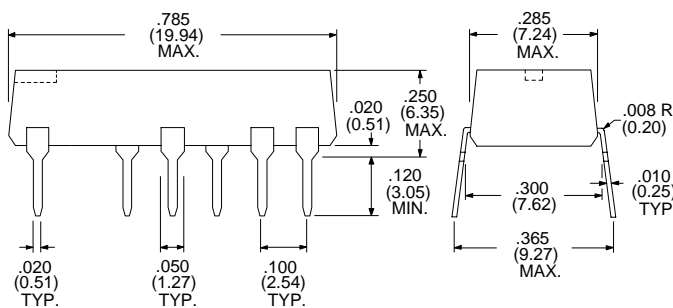
Electrical Specifications at 25°C

74F 5-Tap 14-Pin DIP	74F 5-Tap 8-Pin SIP	Tap Delay Tolerances +/- 5% or 2ns					Tap-to-Tap (ns)
		Tap 1	Tap 2	Tap 3	Tap 4	Tap 5	
FAIDM-7	FSIDM-7	3.0	4.0	5.0	6.0	7 ± 1.0	** 1.0 ± 0.4
FAIDM-9	FSIDM-9	3.0	4.5	6.0	7.5	9 ± 1.0	** 1.5 ± 0.5
FAIDM-11	FSIDM-11	3.0	5.0	7.0	9.0	11 ± 1.0	** 2.0 ± 0.7
FAIDM-13	FSIDM-13	3.0	5.5	8.0	10.5	13 ± 1.5	** 2.5 ± 1.0
FAIDM-15	FSIDM-15	3.0	6.0	9.0	12.0	15 ± 1.5	3 ± 1.0
FAIDM-20	FSIDM-20	4.0	8.0	12.0	16.0	20 ± 2.0	4 ± 1.5
FAIDM-25	FSIDM-25	5.0	10.0	15.0	20.0	25 ± 2.0	5 ± 2.0
FAIDM-30	FSIDM-30	6.0	12.0	18.0	24.0	30 ± 2.0	6 ± 2.0
FAIDM-35	FSIDM-35	7.0	14.0	21.0	28.0	35 ± 2.0	7 ± 2.0
FAIDM-40	FSIDM-40	8.0	16.0	24.0	32.0	40 ± 2.0	8 ± 2.0
FAIDM-45	FSIDM-45	9.0	18.0	27.0	36.0	45 ± 2.25	9 ± 2.0
FAIDM-50	FSIDM-50	10.0	20.0	30.0	40.0	50 ± 2.50	10 ± 2.0
FAIDM-60	FSIDM-60	12.0	24.0	36.0	48.0	60 ± 3.0	12 ± 2.0
FAIDM-75	FSIDM-75	15.0	30.0	45.0	60.0	75 ± 3.75	15 ± 2.5
FAIDM-80	FSIDM-80	16.0	32.0	48.0	64.0	80 ± 4.0	16 ± 2.5
FAIDM-100	FSIDM-100	20.0	40.0	60.0	80.0	100 ± 5.0	20 ± 3.0
FAIDM-125	FSIDM-125	25.0	50.0	75.0	100.0	125 ± 6.25	25 ± 3.0
FAIDM-150	FSIDM-150	30.0	60.0	90.0	120.0	150 ± 7.5	30 ± 3.0
FAIDM-200	FSIDM-200	40.0	80.0	120.0	160.0	200 ± 10.0	40 ± 4.0
FAIDM-250	FSIDM-250	50.0	100.0	150.0	200.0	250 ± 12.5	50 ± 5.0
FAIDM-300	FSIDM-300	60.0	120.0	180.0	240.0	300 ± 15.0	60 ± 6.0
FAIDM-350	FSIDM-350	70.0	140.0	210.0	280.0	350 ± 17.5	70 ± 7.0
FAIDM-400	----	80.0	160.0	240.0	160.0	400 ± 20.0	80 ± 8.0
FAIDM-500	----	100.0	200.0	300.0	400.0	500 ± 25.0	100 ± 10

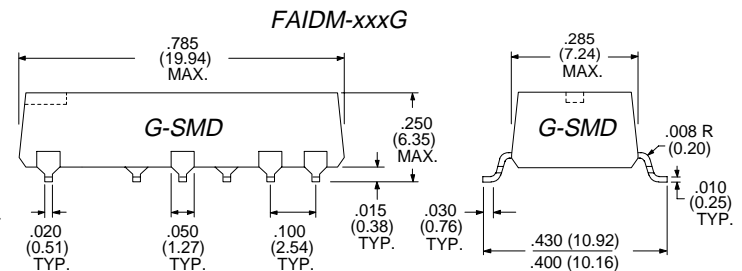
Dimensions in Inches (mm)



FAIDM Series 14-Pin DIP Package



FAIDM Series 14-Pin Gullwing-SMD per Table above add "G" suffix to P/N



Specifications subject to change without notice.

For other values & Custom Designs, contact factory.

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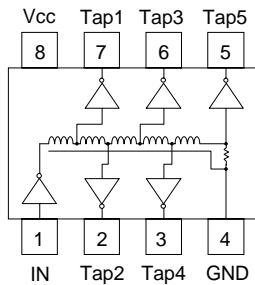
FAX: (714) 896-0971

ACMDM Series Advanced CMOS Logic Buffered 5-Tap Delay Modules

74ACT type input is compatible with TTL . Outputs can Source / Sink 24 mA

- Low Profile 8-Pin Package
Two Surface Mount Versions
- Available in Low Voltage CMOS
74LVC Logic version LVMDM Series
- 5 Equal Delay Taps
- Operating Temp. -40°C to +85°C

ACMDM 8-Pin Schematic



Electrical Specifications at 25°C

74ACT 5 Tap 8-Pin DIP P/N	Tap Delay Tolerances +/- 5% or 2ns (+/- 1ns <13ns)					Tap-to-Tap (ns)
	Tap 1	Tap 2	Tap 3	Tap 4	Total - Tap 5	
ACMDM-30	6.0	12.0	18.0	24.0	30 ± 2.0	6 ± 2.0
ACMDM-35	7.0	14.0	21.0	28.0	35 ± 2.0	7 ± 2.0
ACMDM-40	8.0	16.0	24.0	32.0	40 ± 2.0	8 ± 2.0
ACMDM-50	10.0	20.0	30.0	40.0	50 ± 2.5	10 ± 2.0
ACMDM-60	12.0	24.0	36.0	48.0	60 ± 3.0	12 ± 2.0
ACMDM-75	15.0	30.0	45.0	60.0	75 ± 3.75	15 ± 2.5
ACMDM-80	16.0	32.0	48.0	64.0	80 ± 4.0	16 ± 3.0
ACMDM-100	20.0	40.0	60.0	80.0	100 ± 5.0	20 ± 3.0
ACMDM-125	25.0	50.0	75.0	100.0	125 ± 6.25	25 ± 3.0
ACMDM-150	30.0	60.0	90.0	120.0	150 ± 7.5	30 ± 3.0
ACMDM-200	40.0	80.0	120.0	160.0	200 ± 10.0	40 ± 4.0
ACMDM-250	50.0	100.0	150.0	200.0	250 ± 12.5	50 ± 5.0

TEST CONDITIONS -- Advanced CMOS, 74ACT

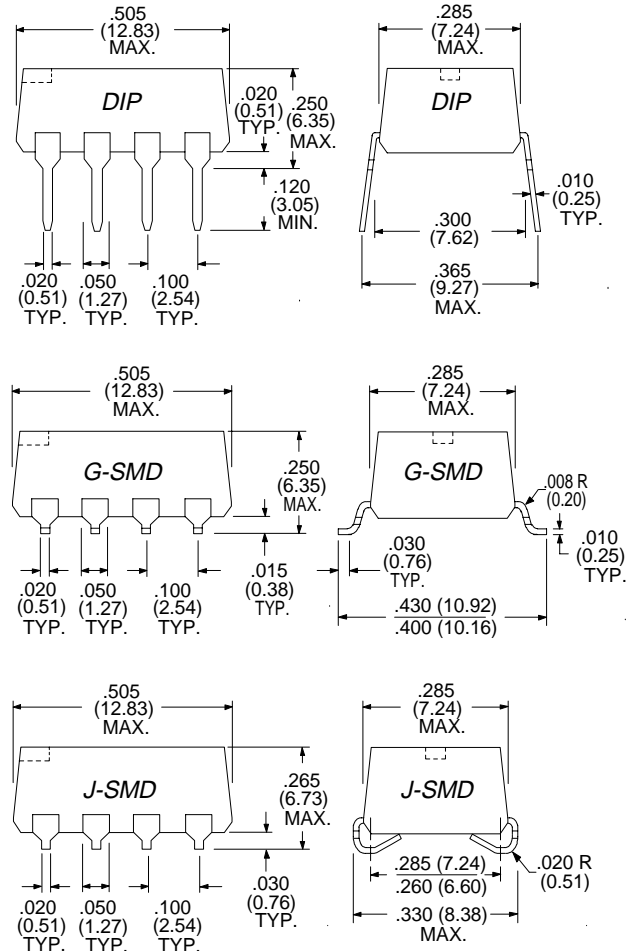
V_{CC} Supply Voltage 5.00VDC
 Input Pulse Voltage 3.00V
 Input Pulse Rise Time 3.0 ns max.
 Input Pulse Width / Period 1000 / 2000 ns

1. Measurements made at 25°C
2. Delay Times measured at 1.50V level of input to +2.50V level of Output on leading edge.
3. Rise Times measured from 10% to 90% points.
4. 50pf probe and fixture load on output under test.

OPERATING SPECIFICATIONS

Supply Voltage, V_{CC} 5.00 ± 0.50 VDC
 Supply Current, I_{CC} 14 mA typ., 28 mA max.
 I_{CCH}, V_{IN} = V_{CC}, V_{CC} = 5.5V 40 µA typ.
 I_{CCL}, V_{IN} = 0V, V_{CC} = 5.5V 25 mA typ.
 Logic "1" Input: V_{IH} 2.00 V min., 5.50V max.
 Logic "0" Input: V_{IL} 0.80 V max.
 Logic "1" Voltage Out, V_{OH} 3.8 V min.
 Logic "0" Voltage Out, V_{OL} 0.44 V max.
 Max. Input Current, I_{IN} ± 1.0 µA
 Minimum Input Pulse Width 40% of Delay min.
 Operating Temperature Range -40° to +85°C
 Storage Temperature Range -65° to +150°C

Dimensions in Inches (mm)



P/N Description

ACMDM - XXX X

74ACT Buffered 5 Tap Delay
Molded Package Series:

8-pin DIP: ACMDM

Total Delay in nanoseconds (ns)

Lead Style: Blank = Thru-hole
 G = "Gull Wing" SMD
 J = "J" Bend SMD

Examples: ACMDM-25G = 25ns (5ns per tap) 74ACT, 8-Pin G-SMD
 ACMDM-100 = 100ns (20ns per tap) 74ACT, 8-Pin DIP

Specifications subject to change without notice.

For other values & Custom Designs, contact factory.

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TEL: (714) 898-0960

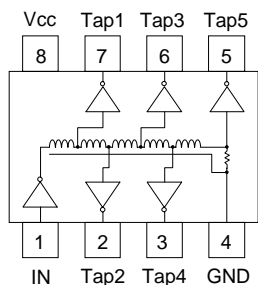
FAX: (714) 896-0971

LVMDM Series LVC Low Voltage Logic Buffered 5-Tap Delay SMD Modules

Inputs accept voltages up to 5.5 V
74LVC type input can be driven from either 3.3V or 5V devices. This allows delay module to serve as a translator in a mixed 3.3V / 5V system environment.

- Low Profile 8-Pin Package
Two Surface Mount Versions
- Low Voltage CMOS 74LVC
Logic Buffered
- 5 Equal Delay Taps
- Operating Temp. -40°C to +85°C

LVMDM 8-Pin Schematic



Electrical Specifications at 25°C

LVC 5 Tap SMD P/N	Tap 1 (ns)	Tap 2 (ns)	Tap 3 (ns)	Tap 4 (ns)	Tap 5 (ns)	Tap-to-Tap (ns)
LVMDM-7G	3.0 ± 1.0	4.0 ± 1.0	5.0 ± 1.0	6.0 ± 1.0	7 ± 1.0	1.0 ± 0.4
LVMDM-9G	3.0 ± 1.0	4.5 ± 1.0	6.0 ± 1.0	7.5 ± 1.0	9 ± 1.0	1.5 ± 0.5
LVMDM-11G	3.0 ± 1.0	5.0 ± 1.0	7.0 ± 1.0	9.0 ± 1.0	11 ± 1.5	2.0 ± 0.6
LVMDM-13G	3.0 ± 1.0	5.5 ± 1.0	8.0 ± 1.0	10.5 ± 1.0	13 ± 1.5	2.5 ± 0.8
LVMDM-15G	3.0 ± 1.0	6.0 ± 1.0	9.0 ± 1.0	12.0 ± 1.5	15 ± 1.5	3.0 ± 1.0
LVMDM-20G	4.0 ± 1.0	8.0 ± 1.2	12.0 ± 1.5	16.0 ± 1.5	20 ± 2.0	4.0 ± 1.0
LVMDM-25G	5.0 ± 1.0	10.0 ± 1.5	15.0 ± 1.5	20.0 ± 2.0	25 ± 2.0	5.0 ± 1.5
LVMDM-30G	6.0 ± 1.0	12.0 ± 1.5	18.0 ± 1.5	24.0 ± 2.0	30 ± 2.0	6.0 ± 1.5
LVMDM-35G	7.0 ± 1.0	14.0 ± 1.5	21.0 ± 2.0	28.0 ± 2.0	35 ± 2.0	7.0 ± 1.8
LVMDM-40G	8.0 ± 1.0	16.0 ± 1.5	24.0 ± 2.0	32.0 ± 2.0	40 ± 2.0	8.0 ± 2.0
LVMDM-45G	9.0 ± 1.0	18.0 ± 1.5	27.0 ± 2.0	36.0 ± 2.0	45 ± 2.25	9.0 ± 2.0
LVMDM-50G	10.0 ± 1.5	20.0 ± 2.0	30.0 ± 2.0	40.0 ± 2.0	50 ± 2.5	10 ± 2.0
LVMDM-60G	12.0 ± 1.5	24.0 ± 2.0	36.0 ± 2.0	48.0 ± 2.4	60 ± 3.0	12 ± 2.0
LVMDM-75G	15.0 ± 2.0	30.0 ± 2.0	45.0 ± 2.25	60.0 ± 3.0	75 ± 3.75	15 ± 2.5
LVMDM-80G	16.0 ± 2.0	32.0 ± 2.0	48.0 ± 2.4	64.0 ± 3.2	80 ± 4.0	16 ± 2.5
LVMDM-100G	20.0 ± 2.0	40.0 ± 2.0	60.0 ± 3.0	80.0 ± 2.0	100 ± 5.0	20 ± 3.0

** These part numbers do not have 5 equal taps. Tap-to-Tap Delays reference Tap 1.

TEST CONDITIONS -- Low Voltage CMOS, LVC

- V_{CC} Supply Voltage 3.30VDC
 Input Pulse Voltage 2.70V
 Input Pulse Rise Time 3.0 ns max.
 Input Pulse Width / Period 1000 / 2000 ns
1. Measurements made at 25°C
 2. Delay Times measured at 1.50V level of leading edge.
 3. Rise Times measured from 0.75V to 2.40V.
 4. 50pf probe and fixture load on output under test.

OPERATING SPECIFICATIONS

- Supply Voltage, V_{CC} 3.3 ± 0.3 VDC
 Supply Current, I_{CC} 10 mA typ., 30 mA max.
 Supply Current, I_{CCL}: V_{IN} = GND 22 mA max.
 Supply Current, I_{CCH}: V_{IN} = V_{CC} 10 µA max.
 Input Voltage, V_I 0 V min., 5.5 V max.
 Logic "1" Input, V_{IH} 2.0 V min.
 Logic "0" Input, V_{IL} 0.8 V max.
 Logic "1" Out, V_{OH}: V_{CC} = 3V & I_{OH} = -24 mA 2.0 V min.
 Logic "0" Out, V_{OL}: V_{CC} = 3V & I_{OL} = 24 mA 0.55 V max.
 Input Capacitance, C_I 5 pF, typ.
 Input Pulse Width, P_{WI} 40% of Delay min.
 Operating Temperature Range -40° to +85°C
 Storage Temperature Range -65° to +150°C

P/N Description

LVMDM - XXX X

LVC Buffered 5 Tap Delay
Molded Package Series:

8-pin DIP: LVMDM

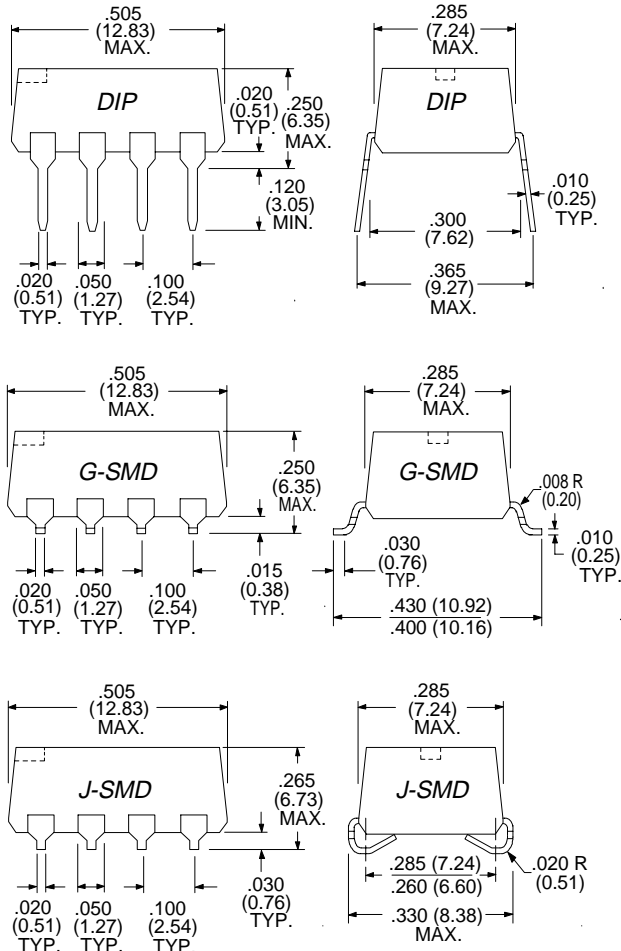
Total Delay in nanoseconds (ns)

Lead Style: Blank = Thru-hole
 G = "Gull Wing" SMD
 J = "J" Bend SMD

Examples: LVMDM-25G = 25ns (5ns per tap) 74LVC, 8-Pin G-SMD

LVMDM-100 = 100ns (20ns per tap) 74LVC, 8-Pin DIP

Dimensions in Inches (mm)



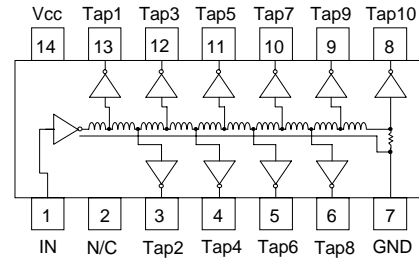
LVITD Series LVC Low Voltage Logic 10-Tap Delay Modules

Inputs accept voltages up to 5.5 V

74LVC type input can be driven from either 3.3V or 5V devices. This allows delay module to serve as a translator in a mixed 3.3V / 5V system environment.

- Operating Temp. -40°C to +85°C
- Low Profile 14-Pin Package
Two Surface Mount Versions
- For 5-Tap 8-Pin Versions see LVMDM Series

LVITD Schematic



Electrical Specifications at 25°C

LVC Logic 10 Tap P/N	Tap Delay Tolerances +/- 5% or 2ns (>15ns +/- 1.0ns)										Tap-to-Tap (ns)
	Tap 1	Tap 2	Tap 3	Tap 4	Tap 5	Tap 6	Tap 7	Tap 8	Tap 9	Total - Tap 10	
LVITD-12	3	4	5	6	7	8	9	10	11	12 ± 2.5	1.0 ± 0.4
LVITD-21	3	5	7	9	11	13	15	17	19	21 ± 2.5	2.0 ± 0.6
LVITD-30	3	6	9	12	15	18	21	24	27	30 ± 2.5	3.0 ± 0.8
LVITD-50	5	10	15	20	25	30	35	40	45	50 ± 2.5	5.0 ± 1.8
LVITD-60	6	12	18	24	30	36	42	48	54	60 ± 3.0	6.0 ± 2.0
LVITD-75	7.5	15	22.5	30	37.5	45	52.5	60	67.5	75 ± 3.75	7.5 ± 2.0
LVITD-80	8	16	24	32	40	48	56	64	72	80 ± 4.0	8.0 ± 2.0
LVITD-100	10	20	30	40	50	60	70	80	90	100 ± 5.0	10.0 ± 2.0
LVITD-125	12.5	25	37.5	50	62.5	75	87.5	100	112.5	125 ± 6.25	12.5 ± 3.0
LVITD-150	15	30	45	60	75	90	105	120	135	150 ± 7.5	15.0 ± 3.0

TEST CONDITIONS -- Low Voltage CMOS, LVC

V_{CC} Supply Voltage 3.30VDC
 Input Pulse Voltage 2.70V
 Input Pulse Rise Time 3.0 ns max.
 Input Pulse Width / Period 1000 / 2000 ns

1. Measurements made at 25°C
2. Delay Times measured at 1.50V level of leading edge.
3. Rise Times measured from 0.75V to 2.40V.
4. 50pf probe and fixture load on output under test.

OPERATING SPECIFICATIONS

Supply Voltage, V_{CC} 3.3 ± 0.3 VDC
 Supply Current, I_{CC} 10 mA typ., 30 mA max.
 Supply Current, I_{CCL}: V_{IN} = GND 22 mA max.
 Supply Current, I_{CCH}: V_{IN} = V_{CC} 10 µA max.
 Input Voltage, V_I 0 V min., 5.5 V max.
 Logic "1" Input, V_{IH} 2.0 V min.
 Logic "0" Input, V_{IL} 0.8 V max.
 Logic "1" Out, V_{OH}: V_{CC} = 3V & I_{OH} = -24 mA 2.0 V min.
 Logic "0" Out, V_{OL}: V_{CC} = 3V & I_{OL} = 24 mA 0.55 V max.
 Input Capacitance, C_I 5 pF, typ.
 Input Pulse Width, P_{WI} 40% of Delay min.
 Operating Temperature Range -40° to +85°C
 Storage Temperature Range -65° to +150°C

P/N Description

LVITD - XXX X

LVC Buffered 10 Tap Delay
 Molded Package Series:

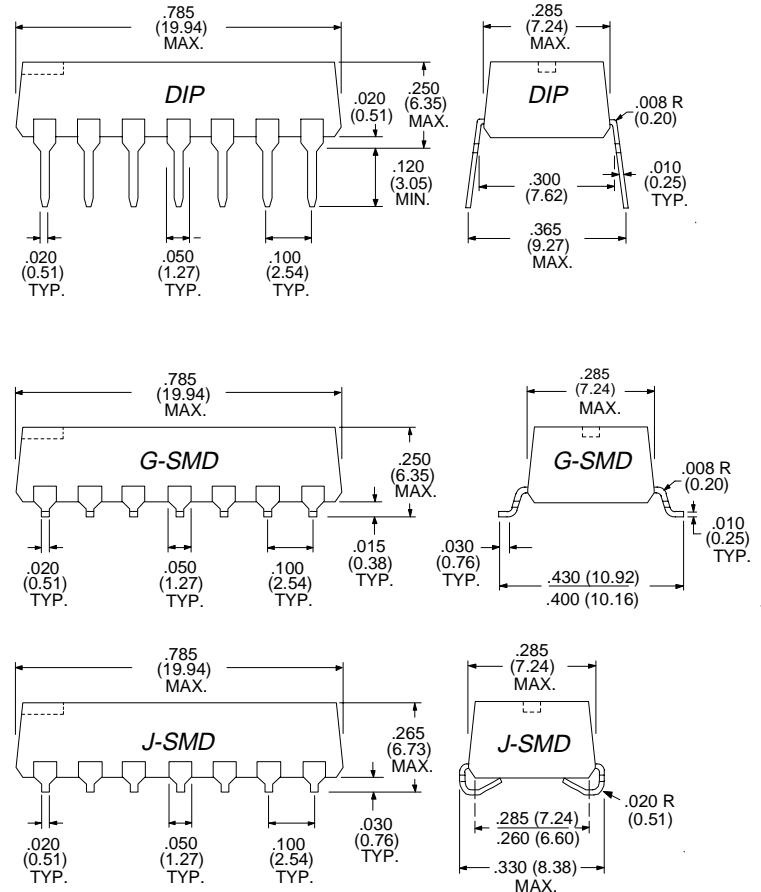
14-pin DIP: LVITD

Total Delay in nanoseconds (ns)

Lead Style: Blank = Thru-hole
 G = "Gull Wing" SMD
 J = "J" Bend SMD

Examples: LVITD-30G = 30ns (3ns per tap) 74LVC, 14-Pin G-SMD
 LVITD-100J = 100ns (10ns per tap) 74LVC, 14-Pin DIP

Dimensions in Inches (mm)



Logic Buffered Single - Dual - Triple Independent Delay Modules

Part Number Description **XXXXX - XXX X**

74ACT -- ACMDL
ACM2D & ACM3D

74F -- FAMDL
FAM2D & FAM3D

74LVC -- LVMDL
LVM2D & LVM3D

Delay Per Line (ns)

Lead Style:
Blank = Auto-Insertable DIP
G = "Gull Wing" Surface Mount
J = "J" Bend Surface Mount

Examples:
FAMDL-4 = 4ns Single 74F, DIP
ACM2D-25G = 25ns Dual ACT, G-SMD
LVM3D-30G = 30ns Triple LVC, G-SMD

GENERAL: For Operating Specifications and Test Conditions refer to corresponding 5-Tap Series FAMDM, ACMDM and LVMDM except Minimum Pulse width and Supply current ratings as below. Delays specified for the Leading Edge.

Operating Temperature Range
FAST/TTL 0°C to +70°C
74ACT -40°C to +85°C
74LVC -40°C to +85°C

Temp. Coefficient of Delay:
Single 500ppm/°C typical
Dual/Triple 800ppm/°C typical

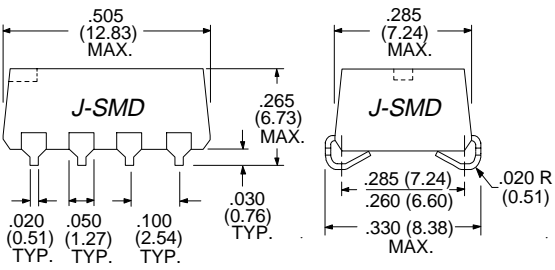
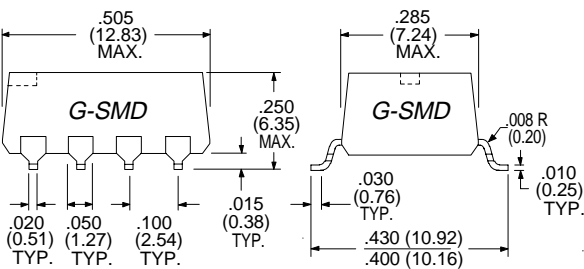
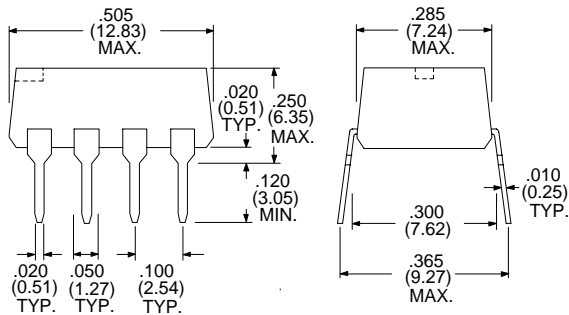
Minimum Input Pulse Width:
Single 40% of total delay
Dual/Triple 100% of total delay

Supply Current, I_{CC} :
FAST/TTL FAMDL 25 mA typ., 48 mA max.
FAM2D 32 mA typ., 65 mA max.
FAM3D 45 mA typ., 95 mA max.

74ACT ACMDL 14 mA typ., 28 mA max.
ACM2D 23 mA typ., 52 mA max.
ACM3D 34 mA typ., 75 mA max.

74LVC LVMDL 10 mA typ., 30 mA max.
LVM2D 15 mA typ., 44 mA max.
LVM3D 21 mA typ., 64 mA max.

Dimensions in Inches (mm)



• FAST / TTL •

Electrical Specifications at 25°C

Delay (ns)	FAST Buffered		
	Single 8-Pin P/N	Dual 8-Pin P/N	Triple 8-Pin P/N
4 ± 1.00	FAMDL-4	FAM2D-4	FAM3D-4
5 ± 1.00	FAMDL-5	FAM2D-5	FAM3D-5
6 ± 1.00	FAMDL-6	FAM2D-6	FAM3D-6
7 ± 1.00	FAMDL-7	FAM2D-7	FAM3D-7
8 ± 1.00	FAMDL-8	FAM2D-8	FAM3D-8
9 ± 1.00	FAMDL-9	FAM2D-9	FAM3D-9
10 ± 1.50	FAMDL-10	FAM2D-10	FAM3D-10
12 ± 1.50	FAMDL-12	FAM2D-12	FAM3D-12
15 ± 1.50	FAMDL-15	FAM2D-15	FAM3D-15
16 ± 1.50	FAMDL-16	FAM2D-16	FAM3D-16
20 ± 2.00	FAMDL-20	FAM2D-20	FAM3D-20
25 ± 2.00	FAMDL-25	FAM2D-25	FAM3D-25
30 ± 2.00	FAMDL-30	FAM2D-30	FAM3D-30
50 ± 2.50	FAMDL-50	---	---
75 ± 3.75	FAMDL-75	---	---
100 ± 5.0	FAMDL-100	---	---

• Advanced CMOS •

Electrical Specifications at 25°C

Delay (ns)	74ACT Adv. CMOS		
	Single 8-Pin P/N	Dual 8-Pin P/N	Triple 8-Pin P/N
6 ± 1.00	ACMDL-6	ACM2D-6	ACM3D-6
7 ± 1.00	ACMDL-7	ACM2D-7	ACM3D-7
8 ± 1.00	ACMDL-8	ACM2D-8	ACM3D-8
9 ± 1.00	ACMDL-9	ACM2D-9	ACM3D-9
10 ± 1.50	ACMDL-10	ACM2D-10	ACM3D-10
12 ± 1.50	ACMDL-12	ACM2D-12	ACM3D-12
15 ± 1.50	ACMDL-15	ACM2D-15	ACM3D-15
16 ± 1.50	ACMDL-16	ACM2D-16	ACM3D-16
20 ± 2.00	ACMDL-20	ACM2D-20	ACM3D-20
25 ± 2.00	ACMDL-25	ACM2D-25	ACM3D-25
30 ± 2.00	ACMDL-30	ACM2D-30	ACM3D-30
50 ± 2.50	ACMDL-50	---	---
75 ± 3.75	ACMDL-75	---	---
100 ± 5.0	ACMDL-100	---	---

• Low Voltage CMOS •

Electrical Specifications at 25°C

Delay (ns)	Low Voltage CMOS Buffered		
	Single 8-Pin P/N	Dual 8-Pin P/N	Triple 8-Pin P/N
4 ± 1.00	LVMDL-4	LVM2D-4	LVM3D-4
5 ± 1.00	LVMDL-5	LVM2D-5	LVM3D-5
6 ± 1.00	LVMDL-6	LVM2D-6	LVM3D-6
7 ± 1.00	LVMDL-7	LVM2D-7	LVM3D-7
8 ± 1.00	LVMDL-8	LVM2D-8	LVM3D-8
9 ± 1.00	LVMDL-9	LVM2D-9	LVM3D-9
10 ± 1.50	LVMDL-10	LVM2D-10	LVM3D-10
12 ± 1.50	LVMDL-12	LVM2D-12	LVM3D-12
15 ± 1.50	LVMDL-15	LVM2D-15	LVM3D-15
16 ± 1.50	LVMDL-16	LVM2D-16	LVM3D-16
20 ± 2.00	LVMDL-20	LVM2D-20	LVM3D-20
25 ± 2.00	LVMDL-25	LVM2D-25	LVM3D-25
30 ± 2.00	LVMDL-30	LVM2D-30	LVM3D-30
50 ± 2.50	LVMDL-50	---	---
75 ± 3.75	LVMDL-75	---	---
100 ± 5.0	LVMDL-100	---	---

Specifications subject to change without notice.

For other values & Custom Designs, contact factory.

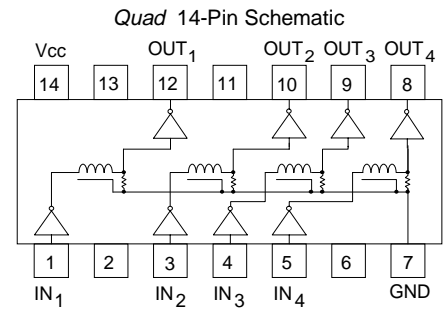
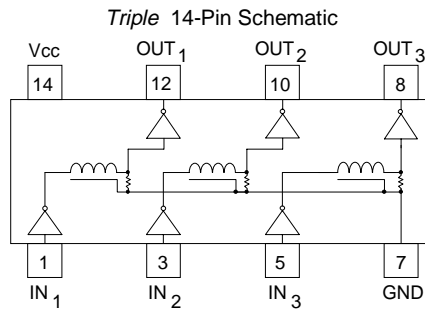
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FAST / TTL Logic Buffered Triple & Quad Delays Modules

Uniform or Various Delays in 14-Pin DIP & SMD Packages

Electrical Specifications at 25°C

Delay (ns)	FAST Buffered Multi-Line Triple P/N	Quadruple P/N
4 ± 1.00	FAI3D-4	FAI4D-4
5 ± 1.00	FAI3D-5	FAI4D-5
6 ± 1.00	FAI3D-6	FAI4D-6
7 ± 1.00	FAI3D-7	FAI4D-7
8 ± 1.00	FAI3D-8	FAI4D-8
10 ± 1.50	FAI3D-10	FAI4D-10
15 ± 2.00	FAI3D-15	FAI4D-15
16 ± 2.00	FAI3D-16	FAI4D-16
20 ± 2.00	FAI3D-20	FAI4D-20
25 ± 2.00	FAI3D-25	FAI4D-25
30 ± 2.00	FAI3D-30	FAI4D-30
50 ± 2.50	FAI3D-50	FAI4D-50



To Specify G-SMD add "G" suffix to P/N

FAI4D-M Series: Variety of Delays per Part
Refer to Delay tolerances for similar delays above

FAST Logic Multi-Line / Multi-Delay P/N	Line 1 (ns) Pin 1 to Pin 12	Line 2 (ns) Pin 3 to Pin 10	Line 3 (ns) Pin 4 to Pin 9	Line 4 (ns) Pin 5 to Pin 8
FAI4D-M01	4.0	5.0	6.0	7.0
FAI4D-M02	4.0	4.0	8.0	8.0
FAI4D-M03	5.0	5.0	10.0	10.0
FAI4D-M04	4.0	6.0	8.0	10.0
FAI4D-M05	6.0	6.0	12.0	12.0
FAI4D-M06	5.0	7.5	10.0	12.5
FAI4D-M07	7.5	7.5	15.0	15.0
FAI4D-M08	8.0	8.0	16.0	16.0
FAI4D-M09	10.0	10.0	20.0	20.0
FAI4D-M10	5.0	5.0	20.0	20.0
FAI4D-M11	10.0	10.0	20.0	20.0
FAI4D-M12	4.0	8.0	16.0	32.0

OPERATING SPECIFICATIONS

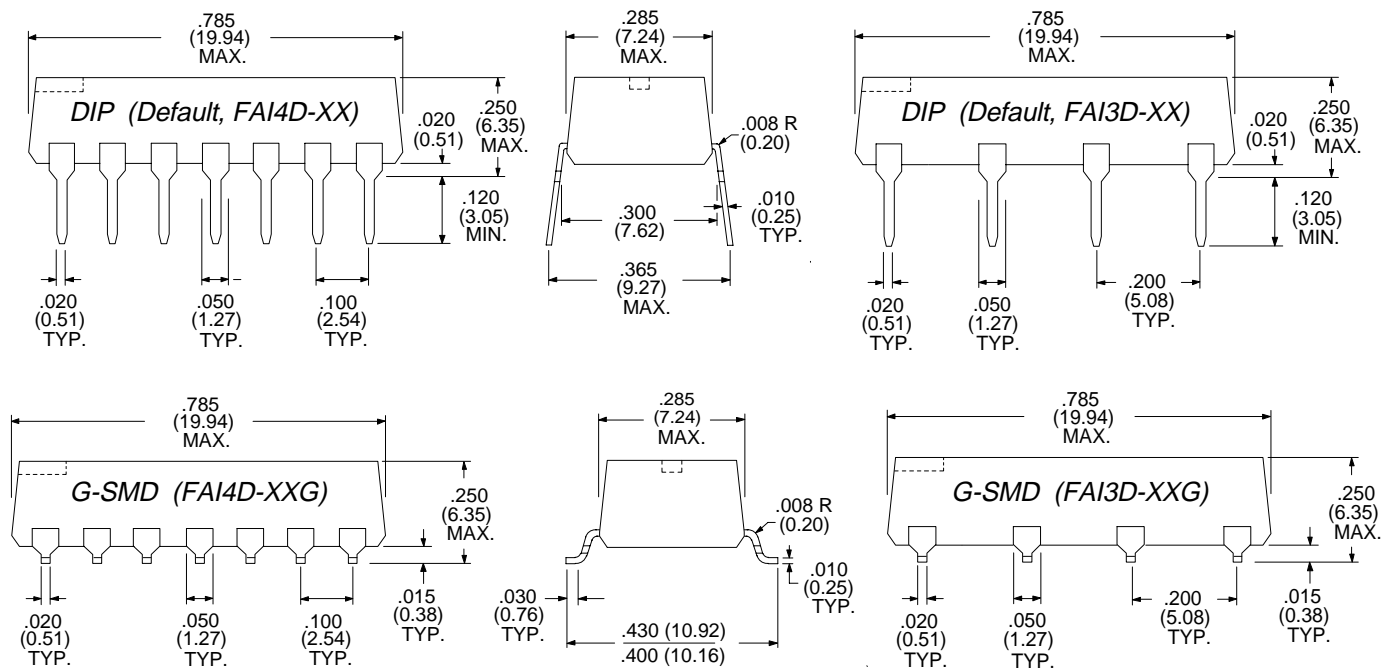
- V_{CC} Supply Voltage 5.00 ± 0.25 VDC
- I_{CC} Supply Current (3D) 45 mA typ., 95 mA max.
- I_{CC} Supply Current (4D) 65 mA typ., 130 mA max.
- Logic "1" Input: V_{IH} 2.00 V min., 5.50 V max.
- I_{IH} 20 µA max. @ 2.70V
- Logic "0" Input: V_{IL} 0.80 V max.
- I_{IL} -0.6 mA max.
- V_{OH} Logic "1" Voltage Out 2.40 V min.
- V_{OL} Logic "0" Voltage Out 0.50 V max.
- P_{wi} Input Pulse Width 100% of Delay
- Operating Temperature Range 0° to 70°C
- Storage Temperature Range -65° to +150°C

TEST CONDITIONS

(Measurements made at 25°C)

- V_{CC} Supply Voltage 5.00VDC
- Input Pulse Voltage 3.20V
- Input Pulse Rise Time 3.0 ns max.
- Input Pulse Period 500 ns
- Input Pulse Width 1000 ns

Dimensions in Inches (mm)



Specifications subject to change without notice.

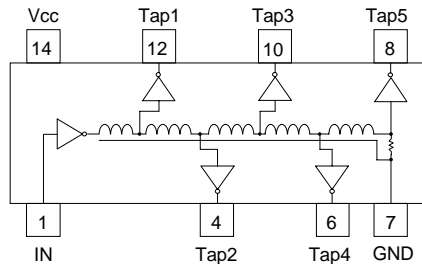
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DTZM Series FAST / TTL Buffered 5-Tap Delay Modules

- 14-Pin Package Commercial and Mil-Grade Versions
- FAST/TTL Logic Buffered
- 5 Equal Delay Taps
- Operating Temperature Ranges 0°C to +70°C, or -55°C to +125°C
- 8-Pin Versions: FAMDM Series SIP Versions: FSIDM Series
- Low Voltage CMOS Versions refer to LVMDM / LVIDM Series

DTZM 14-Pin Schematic



Electrical Specifications at 25°C

TTL Buffered 5 Tap Modules		Tap Delay Tolerances +/- 5% or 2ns (+/- 1ns <13ns)					Tap-to-Tap (ns)
Part Number	Mil-Grade P/N	Tap 1	Tap 2	Tap 3	Tap 4	Total - Tap 5	
DTZM1-9	DTZM3-9M	5.0	6.0	7.0	8.0	9 ± 1.0	** 1.0 ± 0.5
DTZM1-13	DTZM3-13M	5.0	7.0	9.0	11.0	13 ± 1.5	** 2.0 ± 0.8
DTZM1-17	DTZM3-17M	5.0	8.0	11.0	14.0	17 ± 1.5	3.0 ± 1.0
DTZM1-20	DTZM3-20M	4.0	8.0	12.0	16.0	20 ± 1.5	4.0 ± 1.5
DTZM1-25	DTZM3-25M	5.0	10.0	15.0	20.0	25 ± 2.0	5.0 ± 2.0
DTZM1-30	DTZM3-30M	6.0	12.0	18.0	24.0	30 ± 2.0	6.0 ± 2.0
DTZM1-35	DTZM3-35M	7.0	14.0	21.0	28.0	35 ± 2.0	7.0 ± 2.0
DTZM1-40	DTZM3-40M	8.0	16.0	24.0	32.0	40 ± 2.0	8.0 ± 2.0
DTZM1-45	DTZM3-45M	9.0	18.0	27.0	36.0	45 ± 2.25	9.0 ± 2.0
DTZM1-50	DTZM3-50M	10.0	20.0	30.0	40.0	50 ± 2.5	10 ± 2.0
DTZM1-60	DTZM3-60M	12.0	24.0	36.0	48.0	60 ± 3.0	12 ± 2.0
DTZM1-75	DTZM3-75M	15.0	30.0	45.0	60.0	75 ± 3.75	15 ± 2.5
DTZM1-80	DTZM3-80M	16.0	32.0	48.0	64.0	80 ± 4.0	16 ± 2.5
DTZM1-100	DTZM3-100M	20.0	40.0	60.0	80.0	100 ± 5.0	20 ± 3.0
DTZM1-125	DTZM3-125M	25.0	50.0	75.0	100.0	125 ± 6.25	25 ± 3.0
DTZM1-150	DTZM3-150M	30.0	60.0	90.0	120.0	150 ± 7.5	30 ± 3.0
DTZM1-200	DTZM3-200M	40.0	80.0	120.0	160.0	200 ± 10.0	40 ± 4.0
DTZM1-250	DTZM3-250M	50.0	100.0	150.0	200.0	250 ± 12.5	50 ± 5.0
DTZM1-300	DTZM3-300M	60.0	120.0	180.0	240.0	300 ± 15.0	60 ± 6.0
DTZM1-350	DTZM3-350M	70.0	140.0	210.0	280.0	350 ± 17.5	70 ± 7.0
DTZM1-400	DTZM3-400M	80.0	160.0	240.0	320.0	400 ± 20.0	80 ± 8.0
DTZM1-500	DTZM3-500M	100.0	200.0	300.0	400.0	500 ± 25.0	100 ± 10.0
DTZM1-800	DTZM3-800M	160.0	320.0	480.0	640.0	800 ± 40.0	160 ± 16.0

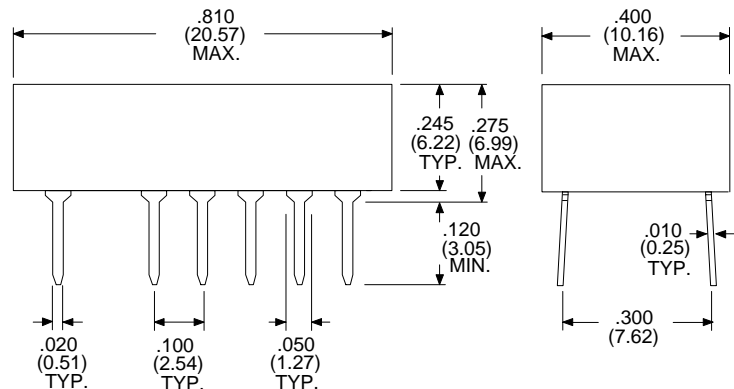
** These part numbers do not have 5 equal taps. Tap-to-Tap Delays reference Tap 1.

TEST CONDITIONS -- FAST / TTL

- V_{CC} Supply Voltage 5.00VDC
 Input Pulse Voltage 3.20V
 Input Pulse Rise Time 3.0 ns max.
 Input Pulse Width / Period 1000 / 2000 ns
1. Measurements made at 25°C
 2. Delay Times measured at 1.50V level of leading edge.
 3. Rise Times measured from 0.75V to 2.40V.
 4. 10pf probe and fixture load on output under test.

Dimensions in Inches (mm)

Commercial Grade 14-Pin Package with Unused Leads Removed as per Schematic. (For Mil-Grade DTZM3 the Height is 0.335")



OPERATING SPECIFICATIONS

- V_{CC} Supply Voltage 5.00 ± 0.25 VDC
 I_{CC} Supply Current 48 mA Maximum
 Logic "1" Input: V_{IH} 2.00 V min., 5.50 V max.
 I_{IH} 20 µA max. @ 2.70V
 Logic "0" Input: V_{IL} 0.80 V max.
 I_{IL} -0.6 mA mA
 V_{OH} Logic "1" Voltage Out 2.40 V min.
 V_{OL} Logic "0" Voltage Out 0.50 V max.
 P_{WI} Input Pulse Width 40% of Delay min.
 Operating Temperature Range 0° to 70°C
 Storage Temperature Range -65° to +150°C

P/N Description

DTZM1 - XXX X

Buffered 5 Tap Delays:

14-pin Com!: DTZM1
 14-pin MIL: DTZM3

Total Delay in nanoseconds (ns)

Temp. Range Blank = Commercial
 M = Mil-Grade

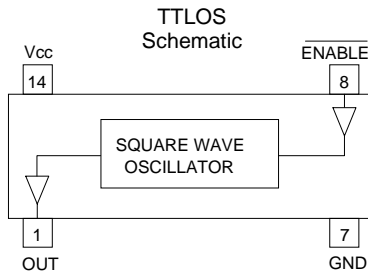
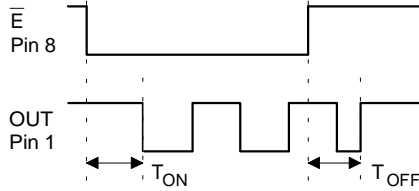
Examples: DTZM1-25 = 25ns (5ns per tap)
 74F, 14-Pin Thru-hole
 DTZM3-50M = 50ns (10ns per tap)
 74F, 14-Pin, Mil-Grade

MIL-GRADE: DTZM3 Military Grade delay lines use integrated circuits screened to MIL-STD-883B with an operating temperature range of -55 to +125°C. These devices have a package height of .335"

*Auto-Insertable DIP and Surface Mount Versions:
 Refer to FAIDM Series, same 14-pin footprint.
 For space saving, refer to FAMDM 8-pin Series*

TTL Gated Oscillators

These gated oscillators permit synchronization of the output square wave with the high-to-low transition of the enable input. When the enable is high, the output is held high. The output will start with a high-to-low transition one half-cycle after the input trigger. The output frequency tolerance is $\pm 3\%$.

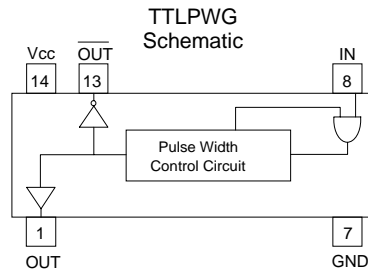
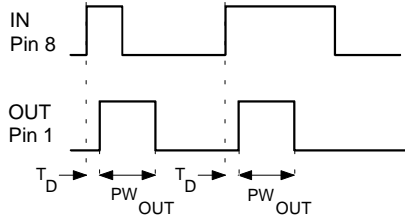


Electrical Specifications at 25°C

TTL Gated Oscillators	
Part Number	Output Frequency
TTLOS-5	5 MHz
TTLOS-10	10 MHz
TTLOS-15	15 MHz
TTLOS-20	20 MHz
TTLOS-25	25 MHz
TTLOS-30	30 MHz
TTLOS-33	33 MHz
TTLOS-35	35 MHz
TTLOS-40	40 MHz
TTLOS-45	45 MHz
TTLOS-50	50 MHz
TTLOS-66	66 MHz
TTLOS-75	75 MHz
TTLOS-80	80 MHz

TTL Pulse Width Generator Modules

Triggered by the input's rising edge (input pulse width 10 ns, min.), a pulse of specified width will be generated at the output with a propagation delay of 5 ± 2 ns (7 ± 2 ns, for inverted output). High-to-low transitions will not trigger the unit. Designed for output duty-cycle less than 50%.

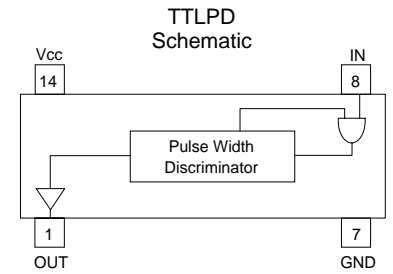
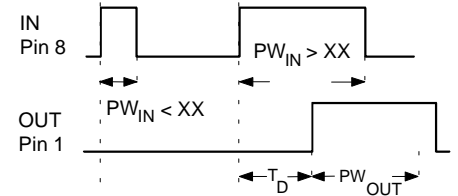


Electrical Specifications at 25°C

TTL Buffered Pulse Width Generator Modules		
Part Number	Output Pulse Width (ns)	Maximum Freq. (MHz)
TTLPWG-5	5 ± 1.0	63
TTLPWG-7	7 ± 1.0	53
TTLPWG-10	10 ± 1.5	42
TTLPWG-15	15 ± 2.0	32
TTLPWG-20	20 ± 2.0	22
TTLPWG-25	25 ± 2.0	19
TTLPWG-30	30 ± 2.0	15
TTLPWG-35	35 ± 2.0	13
TTLPWG-40	40 ± 2.0	11
TTLPWG-45	45 ± 2.25	10
TTLPWG-50	50 ± 2.5	9
TTLPWG-60	60 ± 3.0	8
TTLPWG-80	80 ± 4.0	6
TTLPWG-100	100 ± 5.0	5

TTL Pulse Width Discriminators

Input pulse widths greater than the Nominal value (XX in ns from P/N TTLPD-XX) of the module, will propagate with delay $(XX + 5ns) \pm 5\%$ or 2 ns, whichever is greater. Output pulse width equals input width $\pm 7\%$ or 4 ns, whichever is greater. Input pulse widths less than Nominal value are suppressed.



Electrical Specifications at 25°C

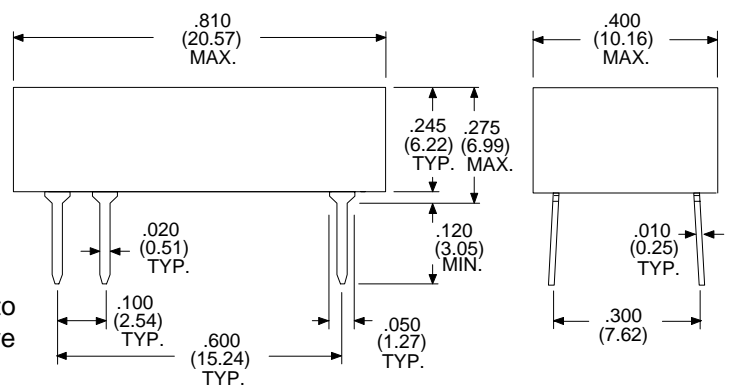
TTL Pulse Width Discriminator Modules		
Part Number	Suppressed Pulse Width, Max. (ns)	Passed Pulse Width, Min. (ns)
TTLPD-10	< 8.5	> 11.5
TTLPD-15	< 13.5	> 16.5
TTLPD-20	< 18.5	> 21.5
TTLPD-25	< 23.5	> 26.5
TTLPD-30	< 28.5	> 31.5
TTLPD-40	< 38.0	> 42.0
TTLPD-50	< 47.5	> 52.5
TTLPD-60	< 57.0	> 63.0
TTLPD-75	< 71.0	> 79.0
TTLPD-100	< 95.0	> 105.0
TTLPD-120	< 114.0	> 126.0
TTLPD-125	< 118.7	> 131.3
TTLPD-150	< 142.5	> 157.5
TTLPD-200	< 190.0	> 210.0

OPERATING SPECIFICATIONS

- V_{CC} Supply Voltage 5.00 \pm 0.25 VDC
- Supply Current, I_{CC}
 - TTLPWG** 35 mA typ., 55 mA max.
 - TTLPD** 42 mA typ., 60 mA max.
 - TTLOS** 15 mA typ., 30 mA max.
- Logic "1" Input: V_{IH} 2.00 V min., 5.50 V max.
- Logic "0" Input: V_{IL} 0.80 V max.
- V_{OH} Logic "1" Voltage Out 2.40 V min.
- V_{OL} Logic "0" Voltage Out 0.50 V max.
- Operating Temperature Range 0° to 70°C
- Storage Temperature Range -65° to +150°C

MIL-GRADE: Add "M" suffix. Integrated circuits screened to MIL-STD-883B with -55 to +125°C operating temperature range. These devices have a package height of .335"

Dimensions in Inches (mm)
14-Pin Package with Unused Leads Removed Per Schematic



Specifications subject to change without notice.

For other values & Custom Designs, contact factory.

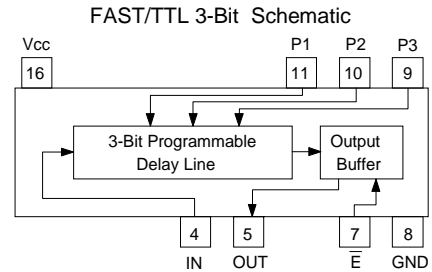
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3-Bit Programmable Delay Modules

PLDM4 Series FAST/TTL Logic

7 Delay Steps -- 4 ns Inherent Delay

Available in Surface Mount



Electrical Specifications at 25°C

3-Bit FAST Part Number	Delay per Step (ns)	Error ref. to 000 (ns)	Initial Delay (ns)	Referenced to "000" - Delay (ns) per Program Setting (P3*P2*P1)							
				000	000	001	010	011	100	101	110
PLDM4-0.5	0.5 ± .25	± .30	4 ± 1.0	0.0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
PLDM4-0.7	0.7 ± .30	± .40	4 ± 1.0	0.0	0.7	1.4	2.1	2.8	3.5	4.2	4.9
PLDM4-0.8	0.8 ± .30	± .50	4 ± 1.0	0.0	0.8	1.6	2.4	3.2	4.0	4.8	5.6
PLDM4-1	1.0 ± .4	± .50	4 ± 1.0	0.0	1.0	2.0	3.0	4.0	5.0	6.0	7.0
PLDM4-1.2	1.2 ± .4	± .60	4 ± 1.0	0.0	1.2	2.4	3.6	4.8	6.0	7.2	8.4
PLDM4-1.25	1.25 ± .5	± .70	4 ± 1.0	0.0	1.25	2.50	3.75	5.00	6.25	7.50	8.75
PLDM4-1.3	1.3 ± .5	± .70	4 ± 1.0	0.0	1.3	2.6	3.9	5.2	6.5	7.8	9.1
PLDM4-1.5	1.5 ± .5	± .70	4 ± 1.0	0.0	1.5	3.0	4.5	6.0	7.5	9.0	10.5
PLDM4-1.8	1.8 ± .6	± .80	4 ± 1.0	0.0	1.8	3.6	5.4	7.2	9.0	10.8	12.6
PLDM4-2	2.0 ± .7	± .80	4 ± 1.0	0.0	2.0	4.0	6.0	8.0	10.0	12.0	14.0
PLDM4-2.5	2.5 ± .7	± .90	4 ± 1.0	0.0	2.5	5.0	7.5	10.0	12.5	15.0	17.5
PLDM4-2.6	2.6 ± .7	± .90	4 ± 1.0	0.0	2.6	5.2	7.8	10.4	13.0	15.6	18.2
PLDM4-3	3.0 ± .7	± 1.0	4 ± 1.0	0.0	3.0	6.0	9.0	12.0	15.0	18.0	21.0

CUMULATIVE TOLERANCES: "Error" Tolerance is for Programmed Delays referenced to Initial Delay, Setting "000." For example, the setting "111" delay of PLDM4-10 is 70.0 ± 3.0ns ref. to "000," and 74.0 ± 4.0ns referenced to the input.

ENABLE input (Pin 7) is active low. Output will be disabled (low) when " \bar{E} " is high.

INPUT FAN-IN: Input, pin 4, is loaded by the internal passive network and 8 gate inputs (74F type). The source driving Pin 4 should be FAST/TTL (74S/74F) type or equivalent, and should not be used to drive any load other than the delay line input.

TEST CONDITIONS -- FAST / TTL

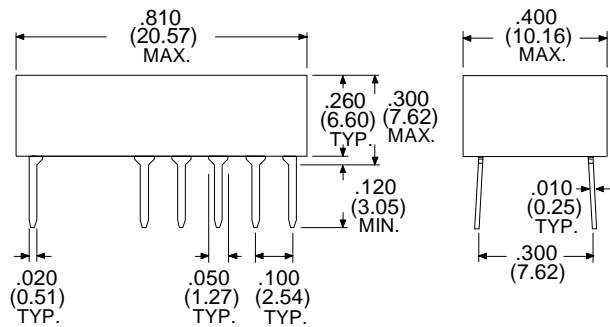
- V_{CC} Supply Voltage 5.00VDC
- Input Pulse Voltage 3.20V
- Input Pulse Rise Time 3.0 ns max.
- Input Pulse Width / Period 1000 / 2000 ns
- 1. Measurements made at 25°C
- 2. Delay Times measured at 1.50V level of leading edge.
- 3. Rise Times measured from 0.75V to 2.40V.
- 4. 10pf probe and fixture load on output.

OPERATING SPECIFICATIONS

- V_{CC} Supply Voltage 5.00 ± 0.25 VDC
- I_{CC} Supply Current 60 mA typ., 80 mA max
- Logic "1" Input *: V_{IH} 2.00 V min., 5.50 V max.
- I_{IH} 50 μA max. @ 2.70V
- Logic "0" Input *: V_{IL} 0.80 V max.
- I_{IL} -0.6 mA mA
- V_{OH} Logic "1" Voltage Out 2.40 V min.
- V_{OL} Logic "0" Voltage Out 0.50 V max.
- P_{WI} Input Pulse Width 40% of Delay min.
- Operating Temperature Range -0° to +70°C
- Storage Temperature Range -65° to +150°C

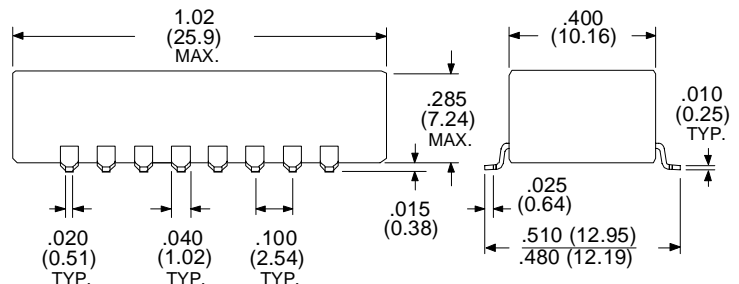
* Refer to "INPUT FAN-IN" note above.
IIL/IIH specified for Programming pins 9, 10 & 11.

Dimensions in Inches (mm)



16-Pin SMD Pkg. Unused leads are NOT removed.

To Specify SMD Package, Add "G" Suffix to P/N
Examples: PLDM4-1.25G, PLDM4-2G

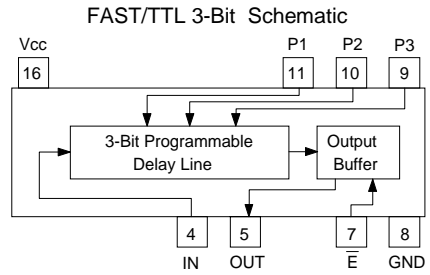


3-Bit Programmable Delay Modules

PLDM7 Series FAST/TTL Logic

7 Delay Steps -- 7 ns Inherent Delay

Available in Surface Mount



Electrical Specifications at 25°C

3-Bit TTL Part Number	Delay per Step (ns)	Error ref. to 000 (ns)	Initial Delay (ns)	Referenced to "000" - Delay (ns) per Program Setting (P3*P2*P1)							
				000	001	010	011	100	101	110	111
PLDM7-1	1.0 ± .4	± .50	7 ± 1.0	0.0	1.0	2.0	3.0	4.0	5.0	6.0	7.0
PLDM7-1.2	1.2 ± .4	± .60	7 ± 1.0	0.0	1.2	2.4	3.6	4.8	6.0	7.2	8.4
PLDM7-1.25	1.25 ± .5	± .70	7 ± 1.0	0.0	1.25	2.5	3.75	5.0	6.25	7.5	8.75
PLDM7-1.3	1.3 ± .5	± .70	7 ± 1.0	0.0	1.3	2.6	3.9	5.2	6.5	7.8	9.1
PLDM7-1.5	1.5 ± .5	± .70	7 ± 1.0	0.0	1.5	3.0	4.5	6.0	7.5	9.0	10.5
PLDM7-1.8	1.8 ± .6	± .80	7 ± 1.0	0.0	1.8	3.6	5.4	7.2	9.0	10.8	12.6
PLDM7-1.9	1.9 ± .7	± .80	7 ± 1.0	0.0	1.9	3.8	5.7	7.6	9.5	11.4	13.3
PLDM7-2	2.0 ± .7	± .80	7 ± 1.0	0.0	2.0	4.0	6.0	8.0	10.0	12.0	14.0
PLDM7-2.5	2.5 ± .7	± .90	7 ± 1.0	0.0	2.5	5.0	7.5	10.0	12.5	15.0	17.5
PLDM7-2.6	2.6 ± .7	± .90	7 ± 1.0	0.0	2.6	5.2	7.8	10.4	13.0	15.6	18.2
PLDM7-3	3.0 ± .7	± 1.0	7 ± 1.0	0.0	3.0	6.0	9.0	12.0	15.0	18.0	21.0
PLDM7-5	5.0 ± 1.0	± 1.5	7 ± 1.0	0.0	5.0	10.0	15.0	20.0	25.0	30.0	35.0
PLDM7-8	8.0 ± 1.2	± 2.5	7 ± 1.0	0.0	8.0	16.0	24.0	32.0	40.0	48.0	56.0
PLDM7-10	10.0 ± 1.5	± 3.0	7 ± 1.0	0.0	10.0	20.0	30.0	40.0	50.0	60.0	70.0

CUMULATIVE TOLERANCES: "Error" Tolerance is for Programmed Delays referenced to Initial Delay, Setting "000." For example, the setting "111" delay of PLDM7-10 is 70.0 ± 3.0ns ref. to "000," and 77.0 ± 4.0ns referenced to the input.

ENABLE input (Pin 7) is active low. Output will be disabled (low) when " \bar{E} " is high.

INPUT FAN-IN: Input, pin 4, is loaded by the internal passive network and 8 gate inputs (74S type). The source driving Pin 4 should be FAST/TTL (74S/74F) type or equivalent, and should not be used to drive any load other than the delay line input.

TEST CONDITIONS -- FAST / TTL

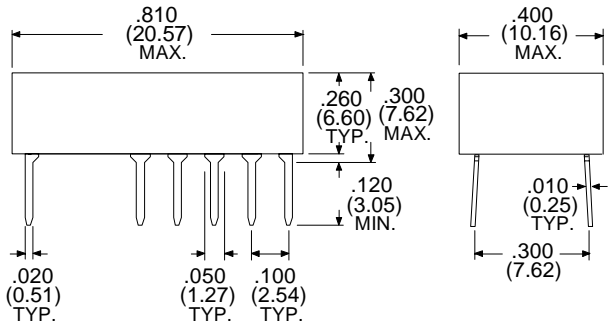
- V_{CC} Supply Voltage 5.00VDC
- Input Pulse Voltage 3.20V
- Input Pulse Rise Time 3.0 ns max.
- Input Pulse Width / Period 1000 / 2000 ns
- 1. Measurements made at 25°C
- 2. Delay Times measured at 1.50V level of leading edge.
- 3. Rise Times measured from 0.75V to 2.40V.
- 4. 10pf probe and fixture load on output.

OPERATING SPECIFICATIONS

- V_{CC} Supply Voltage 5.00 ± 0.25 VDC
- I_{CC} Supply Current 60 mA typ., 80 mA max
- Logic "1" Input *: V_{IH} 2.00 V min., 5.50 V max.
- I_{IH} 50 µA max. @ 2.70V
- Logic "0" Input *: V_{IL} 0.80 V max.
- I_{IL} -2.0 mA mA
- V_{OH} Logic "1" Voltage Out 2.40 V min.
- V_{OL} Logic "0" Voltage Out 0.50 V max.
- P_{WI} Input Pulse Width 40% of Delay min.
- Operating Temperature Range -0° to +70°C
- Storage Temperature Range -65° to +150°C

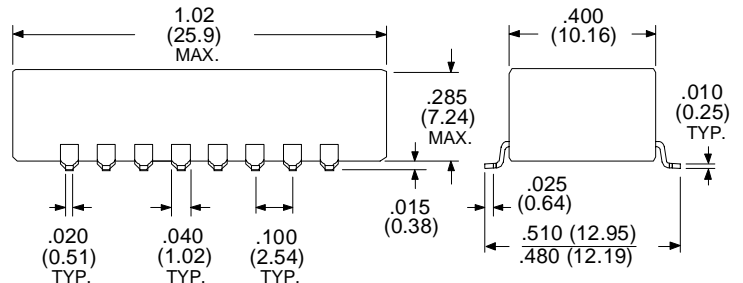
* Refer to "INPUT FAN-IN" note above.
IIL/IH specified for Programming pins 9, 10 & 11.

Dimensions in Inches (mm)



16-Pin SMD Pkg. Unused leads are NOT removed.

To Specify SMD Package, Add "G" Suffix to P/N
Examples: PLDM7-1.25G, PLDM7-2G



10K ECL Logic Buffered Delay 16-Pin Modules

5-Tap: *DECL* • Single: *FECL* • Triple: *MECL*

Electrical Specifications at 25°C

Delay (ns)	Single 10K P/N	Triple 10K P/N
3 ± 0.5	FECL-3	MECL-3
4 ± 0.5	FECL-4	MECL-4
5 ± 0.5	FECL-5	MECL-5
6 ± 0.75	FECL-6	MECL-6
7 ± 0.75	FECL-7	MECL-7
8 ± 0.8	FECL-8	MECL-8
9 ± 1.0	FECL-9	MECL-9
10 ± 1.0	FECL-10	MECL-10
15 ± 1.5	FECL-15	MECL-15
20 ± 1.5	FECL-20	MECL-20
25 ± 1.5	FECL-25	MECL-25
50 ± 2.5	FECL-50	MECL-50
60 ± 3.0	FECL-60	----
75 ± 3.75	FECL-75	----
100 ± 5.0	FECL-100	----

Electrical Specifications at 25°C

10K ECL 5 Tap P/N	Tap Delay Tolerances +/- 5% or 1.5ns (+/- 0.8ns <10ns)					Tap-to-Tap (ns)
	Tap 1	Tap 2	Tap 3	Tap 4	Total - Tap 5	
DECL-6	2.0	3.0	4.0	5.0	6 ± 0.8	** 1 ± 0.4
DECL-10	2.0	4.0	6.0	8.0	10 ± 1.0	2 ± 0.6
DECL-15	3.0	6.0	9.0	12.0	15 ± 1.5	3 ± 0.8
DECL-20	4.0	8.0	12.0	16.0	20 ± 1.5	4 ± 1.0
DECL-25	5.0	10.0	15.0	20.0	25 ± 1.5	5 ± 1.0
DECL-30	6.0	12.0	18.0	24.0	30 ± 1.5	6 ± 1.5
DECL-40	8.0	16.0	24.0	32.0	40 ± 2.0	8 ± 2.0
DECL-45	9.0	18.0	27.0	36.0	45 ± 2.25	9 ± 2.0
DECL-50	10.0	20.0	30.0	40.0	50 ± 2.5	10 ± 2.0
DECL-75	15.0	30.0	45.0	60.0	75 ± 3.75	15 ± 2.5
DECL-100	20.0	40.0	60.0	80.0	100 ± 5.0	20 ± 3.0
DECL-125	25.0	50.0	75.0	100.0	125 ± 6.25	25 ± 3.0
DECL-150	30.0	60.0	90.0	120.0	150 ± 7.5	30 ± 3.0
DECL-200	40.0	80.0	120.0	160.0	200 ± 10.0	40 ± 4.0
DECL-250	50.0	100.0	150.0	200.0	250 ± 12.5	50 ± 5.0

** This part numbers does not have 5 equal taps.
Specified Tap-to-Tap Delays are referenced to Tap 1.

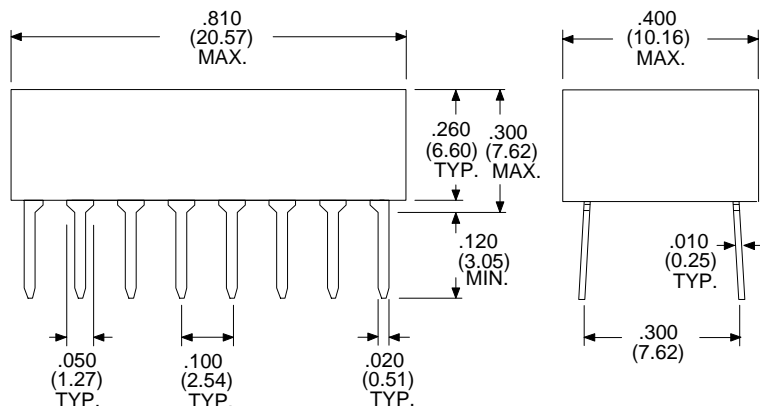
OPERATING SPECIFICATIONS (10K ECL)

V_{EE} Supply Voltage -5.20 ± 0.25 VDC
 Supply Current, I_{EE} , **DECL** 60 mA typ., 75 mA max.
 Supply Current, I_{EE} , **FECL** 40 mA typ., 65 mA max.
 Supply Current, I_{EE} , **MECL** 85 mA typ., 105 mA max.
 Logic "1" Input: V_{IH} -0.98 V min.
 I_{IH} 265 μ A max.
 Logic "0" Input: V_{IL} -1.63 V max.
 I_{IL} 0.5 mA max.
 V_{OH} Logic "1" Voltage Out -0.96 V min.
 V_{OL} Logic "0" Voltage Out -1.65V max.
 T_{RO} Output Rise Time < 3.00 ns typ.
 Input Pulse Width, P_{WI} (**DECL, FECL**) 40% of total delay, min.
 Input Pulse Width, P_{WI} (**MECL**) 100% of total delay, min.
 Operating Temperature Range -30° to +85°C
 Storage Temperature Range -65° to +150°C

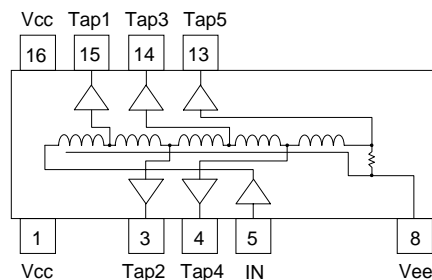
TEST CONDITIONS (Measurements made at 25°C)

V_{EE} Supply Voltage -5.20VDC
 Input Pulse Voltage -0.80V to -1.80V
 Input Pulse Rise Time 3.00ns max.
 Input Pulse Period 4.0 x Total Delay
 Input Pulse Duty Cycle 50%
 Outputs terminated through 100 Ω to -2.00 Vdc.

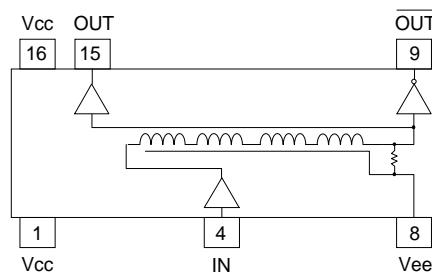
Dimensions in Inches (mm) -- Unused Leads Removed Per Schematic



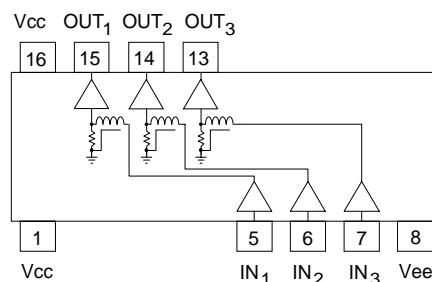
DECL Style Schematic



FECL Style Schematic



MECL Style Schematic



Also Available in 10KH ECL Versions: DECLH, FECLH & MECLH Series

Specifications subject to change without notice.

For other values & Custom Designs, contact factory.

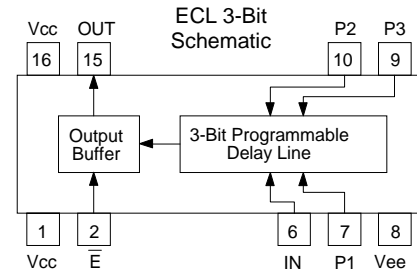
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3-Bit Programmable Delay Modules

PECL3 Series 10K ECL Logic

3PECLH Series 10KH ECL Logic

Available in Surface Mount



ENABLE input \bar{E} , Pin 2, is active low.
Output is disabled (low) when Pin 2 is logic high.

Electrical Specifications at 25°C

3Bit 10K ECL DIP Part Number	3-Bit 10KH ECL DIP Part Number	Delay per Step (ns)	Error ref. to "000" (ns)	Referenced to "000" - Delay (ns) per Program Setting (P3*P2*P1)									
				000	001	010	011	100	101	110	111		
"000"=3±0.5ns **	"000"=1.5±.5ns **												
PECL3-0.5	3PECLH-0.5	0.5 ± .25	± .30	0.0	0.5	1.0	1.5	2.0	2.5	3.0	3.5		
PECL3-0.75	3PECLH0.75	0.75 ± .3	± .50	0.0	0.75	1.50	2.25	3.00	3.75	4.50	5.25		
PECL3-1	3PECLH-1	1.0 ± .4	± .50	0.0	1.0	2.0	3.0	4.0	5.0	6.0	7.0		
PECL3-1.25	3PECLH1.25	1.25 ± .5	± .70	0.0	1.25	2.50	3.75	5.00	6.25	7.50	8.75		
PECL3-1.5	3PECLH-1.5	1.5 ± .5	± .70	0.0	1.5	3.0	4.5	6.0	7.5	9.0	10.5		
PECL3-2	3PECLH-2	2.0 ± .7	± .80	0.0	2.0	4.0	6.0	8.0	10.0	12.0	14.0		
PECL3-2.5	3PECLH-2.5	2.5 ± .7	± .90	0.0	2.5	5.0	7.5	10.0	12.5	15.0	17.5		
PECL3-3	3PECLH-3	3.0 ± .7	± 1.0	0.0	3.0	6.0	9.0	12.0	15.0	18.0	21.0		
PECL3-5	3PECLH-5	5.0 ± 1.0	± 1.5	0.0	5.0	10.0	15.0	20.0	25.0	30.0	35.0		
PECL3-10	3PECLH-10	10.0 ± 1.5	± 3.0	0.0	10.0	20.0	30.0	40.0	50.0	60.0	70.0		

**** INITIAL DELAY & CUMULATIVE TOLERANCES:** "Error" Tolerance is for Programmed Delays Referenced to Initial Delay, Setting "000."
For example, the setting "111" delay of PECL3-2 is 14.0 ± 0.8 ns ref. to "000," and 17.0 ± 1.3 ns referenced to the input,
and the setting "111" delay of 3PECLH-2 is 14.0 ± 0.8 ns ref. to "000," and 15.5 ± 1.3 ns referenced to the input.

INPUT LOADING: Input, Pin 6, internally connected to eight ECL gate inputs terminated by Thevenin equivalent of 100 Ohms to -2V.

OPERATING SPECIFICATIONS (10K, PECL3)

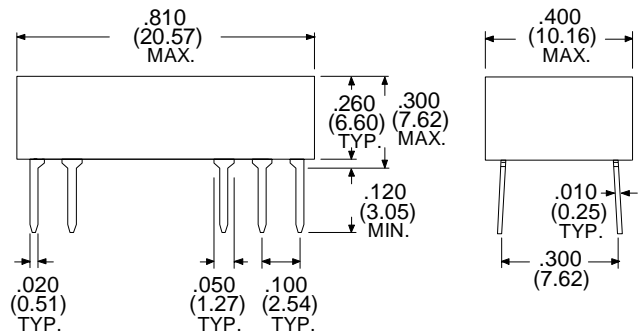
V_{EE} Supply Voltage	-5.20 ± 0.25VDC
I_{EE} Supply Current	60 mA typical
Logic "1" Input: V_{IH}	-0.98V min.
I_{IH}	265 µA max.
I_{IH} (Pin 6) *	-11mA typ.
Logic "0" Input: V_{IL}	-1.63V max.
I_{IL}	0.5 µA min.
I_{IL} (Pin 6) *	-2mA typ.
V_{OH} Logic "1" Voltage Out	-0.96V min.
V_{OL} Logic "0" Voltage Out	-1.65V max.
P_{WI} Input Pulse Width	40% of Max. Delay min.
Operating Temp. Range (10K, PECL3)	-30 to +85°C
Storage Temperature Range	-65 to +150°C

OPERATING SPECIFICATIONS (10KH, 3PECLH)

V_{EE} Supply Voltage	-5.20 ± 0.25VDC
I_{EE} Supply Current	75 mA typical
Logic "1" Input: V_{IH}	-0.98V min.
I_{IH}	320 µA max.
I_{IH} (Pin 6) *	-11mA typ.
Logic "0" Input: V_{IL}	-1.63V max.
I_{IL}	0.7 µA min.
I_{IL} (Pin 6) *	-2mA typ.
V_{OH} Logic "1" Voltage Out	-0.96V min.
V_{OL} Logic "0" Voltage Out	-1.65V max.
P_{WI} Input Pulse Width	40% of Max. Delay min.
Operating Temp. Range (10KH, 3PECLH)	-0 to +75°C
Storage Temperature Range	-65 to +150°C

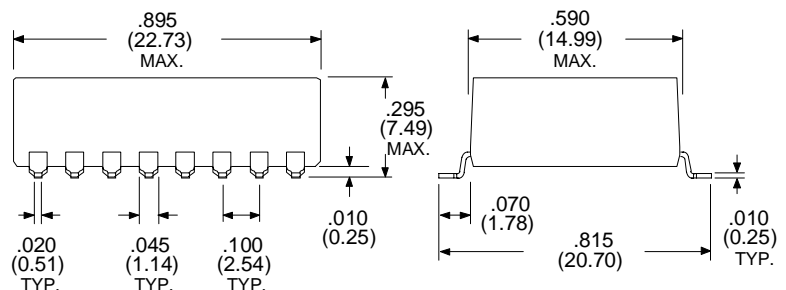
* Refer to Input (Pin 6) Loading note above.

Dimensions in Inches (mm)



16-Pin SMD Pkg. Unused leads are NOT removed.

To Specify SMD Package, Add "H" Suffix to P/N
Examples: PECL3-1.25H, 3PECLH-2H



Specifications subject to change without notice.

For other values & Custom Designs, contact factory.

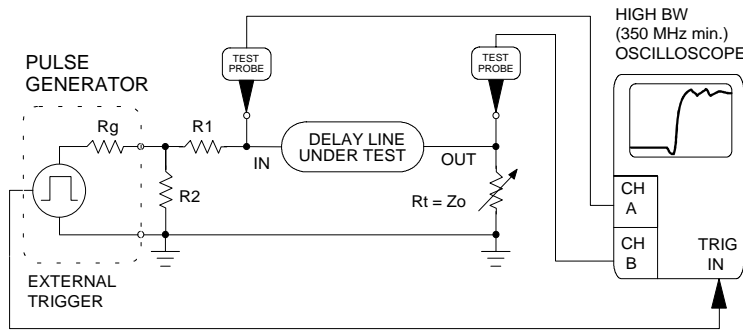
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**Delay Line
Part Number
Index**

Family	Page
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AIZ	6
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AMY	5
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DDECL	**
DECL	26
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DTZM	22
ESP-xxx	**
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TTLOS	23
TTLPD	23
TTLPW	23
TUB	7
TYA	**
TYB	7
TZA	**
TZB	7

** See Website or Contact Rhombus for details.

Test Circuit & Waveform Parameters



R_g = GENERATOR SOURCE IMPEDANCE = 50 OHMS
 R_1, R_2 = INPUT MATCHING PAD RESISTORS
 R_t = TERMINATING RESISTOR
 Z_o = DELAY LINES CHARACTERISTIC IMPEDANCE

$$R_1 = \frac{R_g \times Z_o}{R_2}$$

$$R_2 = \sqrt{\frac{R_g^2 \times Z_o}{Z_o - R_g}}$$

Figure 5A. Recommended test circuit for Passive Delay Lines
 (For Logic Buffered devices no resistors are required)

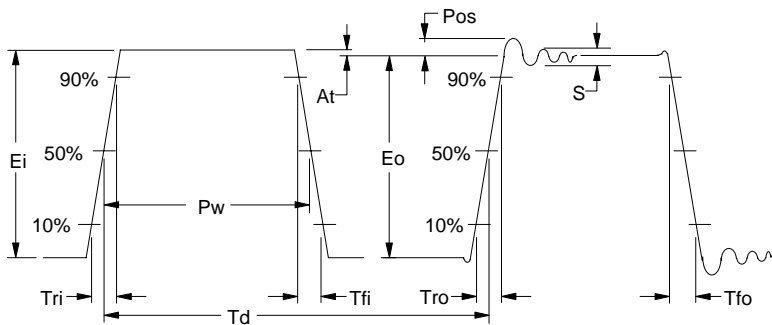


Figure 6A. Passive Delay Line Waveform Parameters

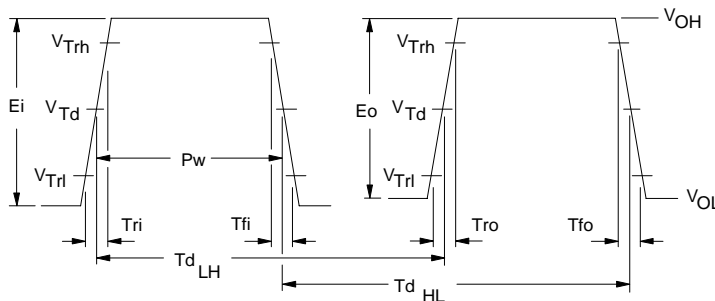


Figure 7A. Active Delay Line Waveform Parameters

**Glossary of
Delay Line Parameters**

Attenuation (At): the difference in peak amplitude between input and output pulses.

D.C. RESISTANCE (DCR): The D.C. resistance, in ohms, measured between the input and output of a delay line.

DELAY TIME (Td): the elapsed time between the respective 50% points on the leading edges of the input and output pulses.

IMPEDANCE (Zo): the effective impedance of the delay line which is equal to the value of the terminating impedance which provides a minimum reflection back to the input of the delay line.

INPUT FALL TIME (Tfi): the elapsed time between the 90% and the 10% points on the trailing edge of the input pulse.

INPUT RISE TIME (Tri): the elapsed time between the 10% and the 90% points on the leading edge of the input pulse.

INPUT VOLTAGE (Ei): the amplitude of the input pulse.

LEADING EDGE: that portion of the pulse which rises from zero to peak amplitude.

OUTPUT RISE TIME (Tfo): the elapsed time between the 10% and the 90% points on the leading edge of the output pulse.

OUTPUT FALL TIME (Tfo): the elapsed time between the 90% and the 10% points on the trailing edge of the output pulse.

OUTPUT VOLTAGE (Eo): the amplitude of the output pulse.

PULSE DISTORTION (S): the magnitude of the largest peak amplitude of all spurious responses in either a positive or negative direction occurring in the period after the top of the leading edge of the output pulse and before two time delays (for flat input pulse top).

PULSE OVERSHOOT (Pos): the peak amplitude of overshoot occurring at the top of the leading edge of the output pulse (for flat input pulse top).

PULSE WIDTH (Pw): the elapsed time between the 50% points on the leading and trailing edge of a pulse.

TRAILING EDGE: that portion of the pulse which falls from peak amplitude to zero.

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