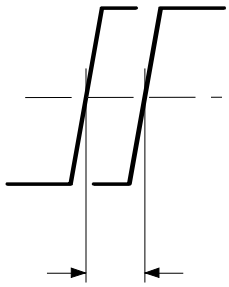
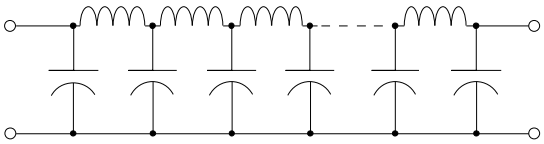
Rhombus
Industries Inc.
Transformers & Magnetic Products



Delay Lines

Electromagnetic



Low Distortion

Fast Rise Times

Single Output

5 - 10 - 20 Taps

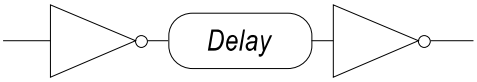
Wide Range of Impedances

50 Ω 100 Ω

75 Ω 200 Ω

93 Ω 500 Ω

Logic Buffered



Buffered Input / Output

5V Logic FAST/TTL

3V Low Voltage CMOS

ECL Logic

Single Output

5 - 10 Taps

Dual / Triple / Quad

Programmables

Pulse Width Control

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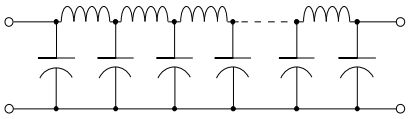
Rhombus Industries Incorporated is a privately owned corporation and a leading designer and manufacturer of transformers and magnetic products. Our headquarters is located in Santa Ana, California and includes engineering, research and development, prototype manufacturing capabilities, sales and extensive in-house testing capabilities. All product is manufactured at our privately owned and operated sub-assembly operation located in Thailand.

Since our founding in 1970, insuring the accuracy, consistency, and overall quality of Rhombus products is of primary concern. All of our products are designed and built to meet the most demanding reliability requirements. We have an extensive quality control program which incorporates statistical process control and is also in strict compliance with MIL-I-45208.

For over 45 years, Rhombus has gained unique experience in providing quality components and innovative designs for users of magnetic products. Rhombus welcomes custom designs tailored to unique customer requirements. Our dedicated employees look forward to proving to you that Rhombus offers the price, delivery and application support advantages that can address your most critical needs.



For Downloadable Catalogs and Data Sheets, as well as, online Magnetic Component resources visit us on the web at

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Pulse & Telecom Transformers

Magnetic Components (Power/SMPS) Inductors & Chokes

Audio Magnetics

Delay Lines

Delay Lines

Passive & Logic Buffered

AIZ Series Passive 10-Tap DIP/SMD Delay Modules

- *Low Profile 14-Pin Package*
  DIP & Surface Mount Versions
- *Low Distortion LC Network*
- *10 Equal Delay Taps, Variety of Footprints*
- *Fast Rise Time -- BW* $\approx 0.35 / t_r$
- *Standard Impedances: 50 - 75 - 100 - 200 Ω*
- *Stable Delay vs. Temperature: 100 ppm/°C*
- *Operating Temperature Range -55°C to +125°C*

Operating Specifications - *Passive Delay Lines*

Pulse Overshoot (Pos)	5% to 10%, typical
Pulse Distortion (S)	3% typical
Working Voltage	25 VDC maximum
Dielectric Strength	100VDC minimum
Insulation Resistance	1,000 MΩ min. @ 100VDC
Temperature Coefficient	70 ppm/°C, typical
Bandwidth (f_C)	0.35/t_r approx.
Operating Temperature Range	-55° to +125°C
Storage Temperature Range	-65° to +150°C

Electrical Specifications at 25°C [1, 2, 3] Note: For Gullwing SMD Package add "G" to P/N in Table

Delay Tolerances		50 Ohm Impedance			75 Ohm Impedance			100 Ohm Impedance			200 Ohm Impedance		
Total (ns)	Tap-to-Tap (ns)	Part Number	Rise Time max. (ns)	DCR max. (Ohms)	Part Number	Rise Time max. (ns)	DCR max. (Ohms)	Part Number	Rise Time max. (ns)	DCR max. (Ohms)	Part Number	Rise Time max. (ns)	DCR max. (Ohms)
5 ± 0.50	0.5 ± 0.2	AIZ-55	1.5	0.8	AIZ-57	1.5	0.8	AIZ-51	1.5	0.8	AIZ-52	1.5	0.8
10 ± 1.00	1.0 ± 0.3	AIZ-105	2.0	0.8	AIZ-107	2.0	1.1	AIZ-101	2.0	1.2	AIZ-102	2.0	1.7
15 ± 1.00	1.5 ± 0.5	AIZ-155	3.0	1.0	AIZ-157	3.0	1.3	AIZ-151	3.0	1.4	AIZ-152	3.3	1.9
20 ± 1.00	2.0 ± 0.5	AIZ-205	4.0	1.2	AIZ-207	4.0	1.5	AIZ-201	4.0	1.6	AIZ-202	4.5	2.4
25 ± 1.25	2.5 ± 0.5	AIZ-255	5.0	1.3	AIZ-257	5.0	1.6	AIZ-251	5.0	1.8	AIZ-252	2.6	3.4
30 ± 1.50	3.0 ± 0.6	AIZ-305	6.0	1.4	AIZ-307	6.0	1.9	AIZ-301	6.0	2.0	AIZ-302	7.2	3.7
35 ± 1.75	3.5 ± 1.0	AIZ-355	7.0	1.5	AIZ-357	7.0	2.6	AIZ-351	7.0	2.9	AIZ-352	8.0	4.0
40 ± 2.00	4.0 ± 1.0	AIZ-405	8.0	1.6	AIZ-407	8.0	2.9	AIZ-401	8.0	3.1	AIZ-402	9.1	4.3
50 ± 2.50	5.0 ± 1.0	AIZ-505	10.0	1.8	AIZ-507	10.0	3.2	AIZ-501	10.0	3.5	AIZ-502	11.0	5.6
60 ± 3.00	6.0 ± 1.5	AIZ-605	12.0	2.0	AIZ-607	12.0	3.5	AIZ-601	12.0	3.8	AIZ-602	12.9	6.1
70 ± 3.50	7.0 ± 1.5	AIZ-705	14.0	2.8	AIZ-707	14.0	4.1	AIZ-701	14.0	4.6	AIZ-702	14.8	6.6
75 ± 3.75	7.5 ± 1.5	AIZ-755	15.0	2.9	AIZ-757	15.0	4.5	AIZ-751	15.0	4.8	AIZ-752	15.7	6.8
80 ± 4.00	8.0 ± 1.8	AIZ-805	16.0	3.0	AIZ-807	16.0	4.8	AIZ-801	16.0	5.0	AIZ-802	16.7	7.0
100 ± 5.00	10.0 ± 2.0	AIZ-1005	20.0	3.4	AIZ-1007	20.0	4.9	AIZ-1001	20.0	5.6	AIZ-1002	21.0	8.2
125 ± 6.25	12.5 ± 2.5	AIZ-1255	25.0	3.8	AIZ-1257	25.0	5.6	AIZ-1251	25.0	6.2	AIZ-1252	25.0	9.5
150 ± 7.50	15.0 ± 3.0	AIZ-1505	30.0	4.8	AIZ-1507	30.0	6.3	AIZ-1501	30.0	6.8	AIZ-1502	30.0	9.8
200 ± 10.00	20.0 ± 3.0	AIZ-2005	40.0	5.7	AIZ-2007	40.0	7.3	AIZ-2001	40.0	7.9	AIZ-2002	40.0	9.9

1. Rise Times are measured from 10% to 90% points.
2. Delay Times measured at 50% point of leading edge.
3. Output (100% Tap) terminated to ground through $R_L=Z_O$

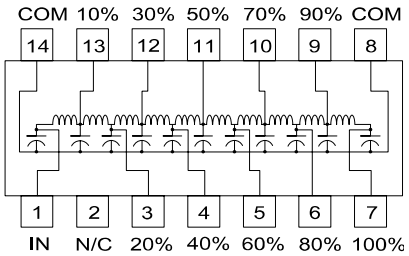
ALTERNATE SCHEMATICS: *Contact factory for identical 10 tap passives available in range of schematic styles*

RoHS Version add suffix "R": AIZ-201GR

*See Similar 10 Tap: "**AIZ**" DIP/SMD, "**TZB**" , "**SIP5**" & "**TF**"*

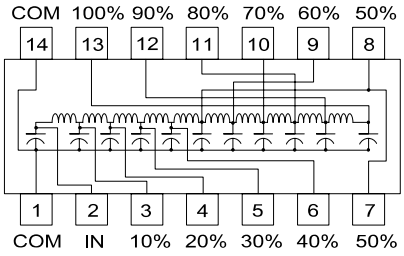
AI**Z** Style Schematic

Most Popular Footprint

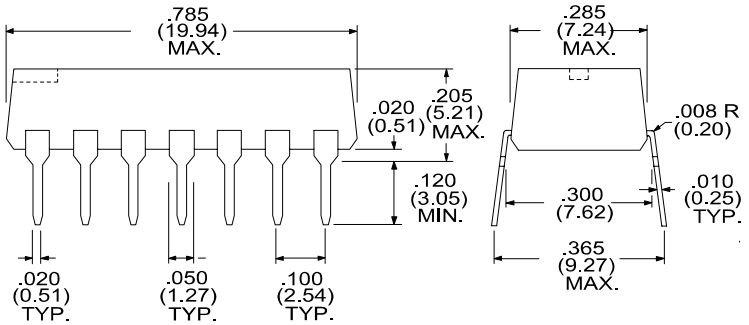


AI**U** Style Schematic

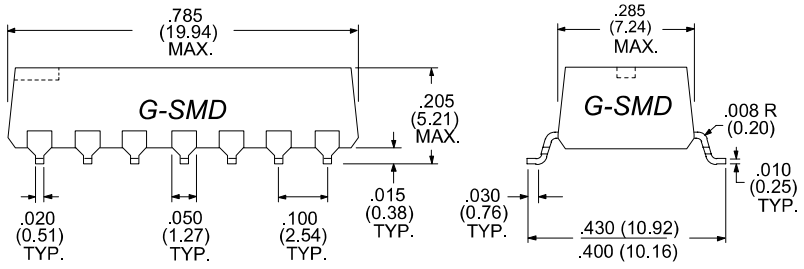
substitute AIU for AIZ in P/N



Dimensions in Inches (mm)



Add "G" Suffix to P/N *Examples: AIZ-51G, AIZ-1505G etc.*



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AMZ & AMY Series Passive 5-Tap DIP/SMD Delay Modules

- *Low Profile 8-Pin Package for Surface Mount Applications*
- *Low Distortion LC Network*
- *5 Equal Delay Taps*
- *Fast Rise Time -- BW* $\approx 0.35 / t_r$
- *Standard Impedances: 50 - 75 - 100 - 200 Ω*
- *Stable Delay vs. Temperature: 100 ppm/°C*
- *Operating Temperature Range -55°C to +125°C*

Operating Specifications - *Passive Delay Lines*

Pulse Overshoot (Pos)	5% to 10%, typical
Pulse Distortion (S)	3% typical
Working Voltage	25 VDC maximum
Dielectric Strength	100VDC minimum
Insulation Resistance	1,000 MΩ min. @ 100VDC
Temperature Coefficient	70 ppm/°C, typical
Bandwidth (f_C)	0.35/t_r approx.
Operating Temperature Range	-55° to +125°C
Storage Temperature Range	-65° to +150°C

Electrical Specifications at 25°C [1, 2, 3] Note: For SMD Package add "G" of "J" as below to P/N in Table

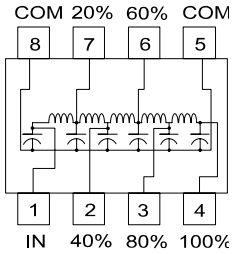
Delay Tolerances Total (ns)	Delay Tolerances Tap-to-Tap (ns)	50 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	75 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	100 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	200 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)
2.5 ± 0.3	0.5 ± 0.2	AMZ-2.55	1.5	0.4	AMZ-2.57	1.5	0.6	AMZ-2.51	1.5	0.6	AMZ-2.52	1.5	0.9
5 ± 0.5	1.0 ± 0.3	AMZ-55	2.0	0.5	AMZ-57	2.0	0.6	AMZ-51	2.0	0.6	AMZ-52	2.0	1.1
6 ± 0.5	1.2 ± 0.4	AMZ-65	2.3	0.5	AMZ-67	2.3	0.6	AMZ-61	2.4	0.7	AMZ-62	2.6	1.1
7 ± 0.5	1.4 ± 0.4	AMZ-75	2.6	0.6	AMZ-77	2.6	0.6	AMZ-71	2.8	0.8	AMZ-72	2.8	1.1
7.5 ± 0.5	1.5 ± 0.5	AMZ-7.55	2.8	0.6	AMZ-7.57	2.8	0.8	AMZ-7.51	2.9	0.8	AMZ-7.52	2.9	1.4
8 ± 0.5	1.6 ± 0.5	AMZ-85	3.0	0.6	AMZ-87	3.0	0.9	AMZ-81	3.0	0.8	AMZ-82	3.1	1.4
9 ± 0.5	1.8 ± 0.5	AMZ-95	3.3	0.7	AMZ-97	3.4	0.9	AMZ-91	3.4	0.8	AMZ-92	3.4	1.4
10 ± 1.0	2.0 ± 0.5	AMZ-105	3.4	0.7	AMZ-107	3.5	0.9	AMZ-101	3.6	0.9	AMZ-102	3.6	1.6
15 ± 1.0	3.0 ± 0.6	AMZ-155	5.2	0.9	AMZ-157	5.2	1.7	AMZ-151	5.2	1.8	AMZ-152	5.2	2.7
20 ± 1.0	4.0 ± 1.0	AMZ-205	6.8	1.0	AMZ-207	6.8	1.9	AMZ-201	6.8	2.0	AMZ-202	6.8	2.8
25 ± 1.25	5.0 ± 1.0	AMZ-255	8.5	1.3	AMZ-257	8.5	2.1	AMZ-251	8.5	2.2	AMZ-252	8.5	3.0
30 ± 1.5	6.0 ± 1.5	AMZ-305	10.2	1.4	AMZ-307	10.2	2.2	AMZ-301	10.2	2.4	AMZ-302	10.2	3.2
35 ± 1.75	7.0 ± 1.5	AMZ-355	11.9	1.5	AMZ-357	11.9	2.4	AMZ-351	11.9	2.6	AMZ-352	11.9	3.4
40 ± 2.0	8.0 ± 1.8	AMZ-405	13.6	1.6	AMZ-407	13.6	2.7	AMZ-401	13.6	2.8	AMZ-402	13.6	3.6
50 ± 2.5	10.0 ± 2.0	AMZ-505	17.0	2.0	AMZ-507	17.0	2.9	AMZ-501	17.0	3.1	AMZ-502	17.0	5.5
60 ± 3.0	12.0 ± 2.5	AMZ-605	20.4	2.2	AMZ-607	20.4	3.3	AMZ-601	20.4	3.3	AMZ-602	20.4	6.2
75 ± 3.75	15.0 ± 3.0	AMZ-755	25.5	2.5	AMZ-757	25.5	3.6	AMZ-751	25.5	3.6	AMZ-752	25.5	6.8
80 ± 4.0	16.0 ± 3.0	AMZ-805	27.2	2.6	AMZ-807	27.2	3.4	AMZ-801	27.2	5.0	AMZ-802	27.2	7.0
100 ± 5.0	20.0 ± 3.0	AMZ-1005	34.0	3.0	AMZ-1007	34.0	3.7	AMZ-1001	34.0	5.8	AMZ-1002	34.0	7.8

1. Rise Times are measured from 10% to 90% points.
2. Delay Times measured at 50% point of leading edge.
3. Output (100% Tap) terminated to ground through $R_L = Z_O$

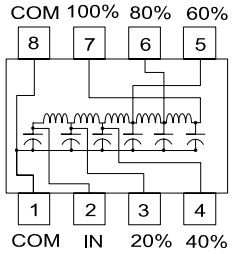
RoHS Version add suffix "R": AMZ-302GR

*See Similar 5 Tap: "**TZA**" & "**SIP4**"*

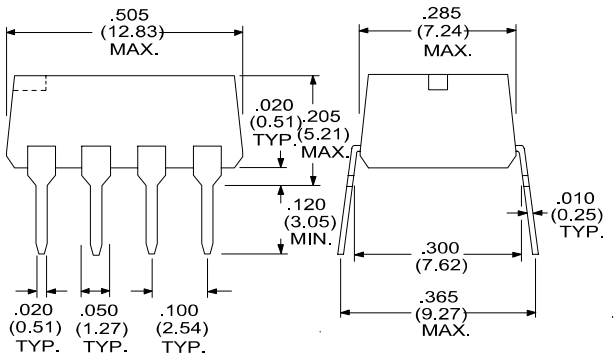
AM**Z** Style Schematic



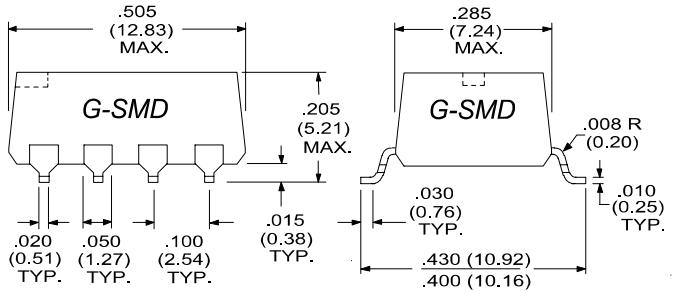
AM**Y** Style Schematic
AMY for AMZ in P/N



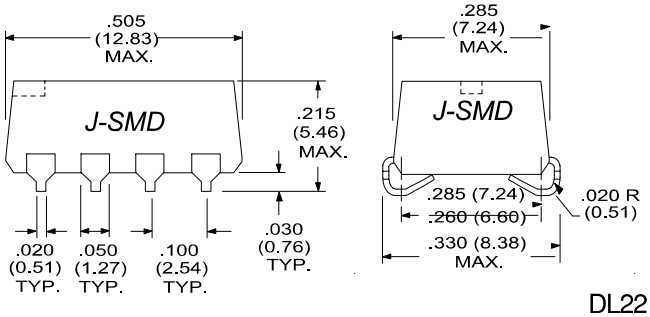
Dimensions in Inches (mm)



To Specify SMD: Add Suffix "G" to P/N



To Specify SMD: Add Suffix "J" to P/N



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AML1 Series *Mini 16-Pin 50-mil SMD Passive Delay Modules*

- *Low Profile 16-Pin 50-mil Package for Surface Mount Applications*
- *Low Distortion LC Network*
- *Fast Rise Time*
- *Standard Impedances: 50 - 75 - 100 - 200 Ω*
- *Stable Delay vs. Temperature: 100 ppm/°C*
- *Operating Temperature Range -55°C to +125°C*

Operating Specifications - *Passive Delay Lines*

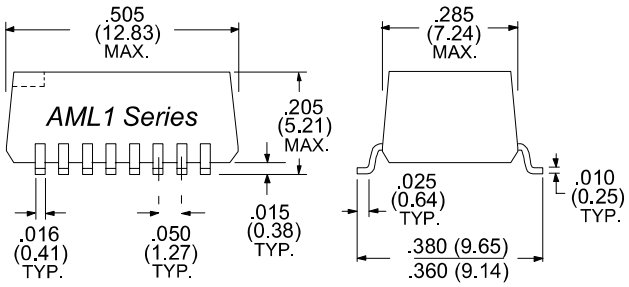
Pulse Overshoot (Pos)	5% to 10%, typical
Pulse Distortion (S)	3% typical
Working Voltage	25 VDC maximum
Dielectric Strength	100VDC minimum
Insulation Resistance	1,000 MΩ min. @ 100VDC
Temperature Coefficient	70 ppm/°C, typical
Bandwidth (f_C)	0.35/t_r approx.
Operating Temperature Range	-55° to +125°C
Storage Temperature Range	-65° to +150°C

Electrical Specifications at 25°C [1, 2, 3]

Delay (ns)	Rise Time 20% - 80% max. (ns)	DCR max. (Ohms)	50 Ohm Part Number	75 Ohm Part Number	100 Ohm Part Number	200 Ohm Part Number
1.0 ± .20	1.6	.20	AML1-1-50	AML1-1-75	AML1-1-10	AML1-1-20
1.5 ± .20	1.6	.30	AML1-1P5-50	AML1-1P5-75	AML1-1P5-10	AML1-1P5-20
2.0 ± .20	1.6	.40	AML1-2-50	AML1-2-75	AML1-2-10	AML1-2-20
2.5 ± .20	1.6	.50	AML1-2P5-50	AML1-2P5-75	AML1-2P5-10	AML1-2P5-20
3.0 ± .20	1.7	.60	AML1-3-50	AML1-3-75	AML1-3-10	AML1-3-20
4.0 ± .20	1.7	.70	AML1-4-50	AML1-4-75	AML1-4-10	AML1-4-20
5.0 ± .25	1.8	.80	AML1-5-50	AML1-5-75	AML1-5-10	AML1-5-20
6.0 ± .30	2.0	.85	AML1-6-50	AML1-6-75	AML1-6-10	AML1-6-20
7.0 ± .30	2.2	.90	AML1-7-50	AML1-7-75	AML1-7-10	AML1-7-20
8.0 ± .30	2.4	.95	AML1-8-50	AML1-8-75	AML1-8-10	AML1-8-20
9.0 ± .30	2.6	1.10	AML1-9-50	AML1-9-75	AML1-9-10	AML1-9-20
10 ± .30	2.8	1.20	AML1-10-50	AML1-10-75	AML1-10-10	AML1-10-20
12 ± .50	3.2	1.50	AML1-12-50	AML1-12-75	AML1-12-10	AML1-12-20
15 ± .70	3.8	1.70	AML1-15-50	AML1-15-75	AML1-15-10	AML1-15-20
20 ± 1.0	4.8	2.00	AML1-20-50	AML1-20-75	AML1-20-10	AML1-20-20

1. Rise Times are measured from 20% to 80% points.
2. Delay Times measured at 50% point of leading edge.
3. Output (100% Tap) terminated to ground through $R_L=Z_O$

Dimensions in Inches (mm)



P/N Description ***AML1* -XX - *XX***

Passive SMD Molded
16-pin 50-mil Delay Modules

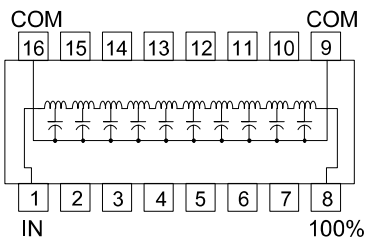
Delay Coding Number
Per Table above

Impedanc Specifier:
50 Ohms = 50
75 Ohms = 75
100 Ohms = 10
200 Ohms = 20

Part Number Examples:
AML1-10-10 = 10 ns, 100 Ω
AML1-25-7 = 25 ns 75 Ω
AML1-6-50 = 6 ns, 50 Ω

RoHS Version add suffix "R": AML1-5-10R

AML1 Schematic



SH6G Series Mini 6-Pin SMD Passive Delay Modules

- Small Gullwing SMD Package
- Fast Rise Time, Low DCR
- Low Distortion LC Network
- Tight Delay Tolerance

- *Standard Impedances: 50 to 100 Ω*
  Contact factory for 200 Ω Impedance versions
- *Stable Delay vs. Temperature: 100 ppm/°C*
- *Operating Temperature Range -55°C to +125°C*

Electrical Specifications at 25°C [1, 2, 3, 4]

Delay Code (Refer to P/N description)	Delay Tolerance (ns)	Rise Time (ns)	DCR (ohms)
010	1.0 ± 0.20	0.70	0.35
015	1.5 ± 0.20	0.80	0.35
020	2.0 ± 0.20	0.90	0.35
025	2.5 ± 0.25	1.00	0.40
030	3.0 ± 0.30	1.20	0.40
035	3.5 ± 0.30	1.30	0.45
040	4.0 ± 0.40	1.50	0.45
045	4.5 ± 0.40	1.70	0.45
050	5.0 ± 0.40	1.80	0.50
060	6.0 ± 0.40	2.20	0.55
070	7.0 ± 0.40	2.40	0.55
075	7.5 ± 0.40	2.50	0.60
080	8.0 ± 0.40	2.60	0.75
090	9.0 ± 0.50	2.80	0.75
100	10.0 ± 0.60	3.00	0.75
110	11.0 ± 0.60	3.30	0.75
120	12.0 ± 0.60	3.50	0.75

1. Rise Times are measured from 20% to 80% points.
2. Delay Times measured at 50% points of leading edge.
3. Impedance, Z_O, tolerance ± 10 %
4. Output terminated to ground through $R_L = Z_O$

P/N Description

SH6G XXX X

Passive Single Output
6-pin Delay Module Series

Delay "Code" Per Table

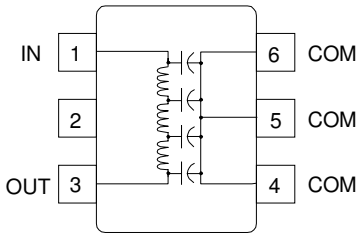
Impedance Specifier:
"5" =50 Ohms, "7" =50 Ohms,
"9" =93 Ohms, "10" = 100 Ohms

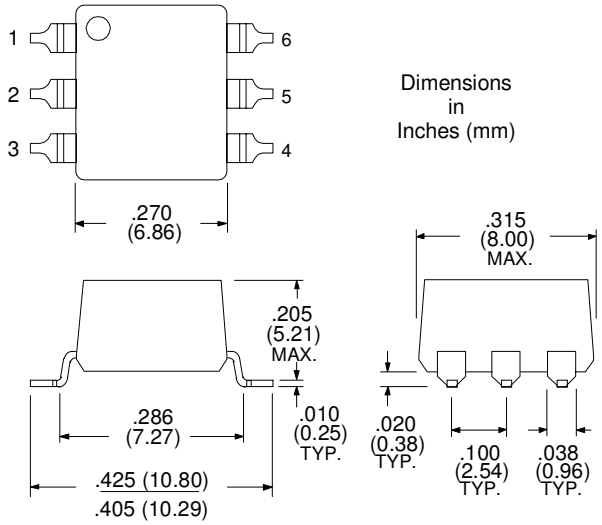
Part Number Examples:

SH6G0155 = 1.5 ns, 50 Ω, 6-pin G-SMD
SH6G1207 = 12 ns, 75 Ω, 6-pin G-SMD
SH6G0259 = 2.5 ns, 93 Ω, 6-pin G-SMD RoHS

Passive Delay Line Parameters	Minimum	Typical	Maximum
Pulse Overshoot (Pos)		10%	
Pulse Distortion (S)		3%	
Working Voltage			25 VDC
Dielectric Strength	100VDC		
Insulation Resistance, @ 100VDC	1,000 MΩ		
Temperature Coefficient		100 ppm/ C	
Bandwidth, approx. (fc)		0.35/tr	
Operating Temperature Range	-55 C		+125 C
Storage Temperature Range	-65 C		+155 C

Schematic Diagram





Dimensions in Inches (mm)

RoHS Compliant Version

To Order RoHS Version add suffix "R":

Standard P/N	RoHS Version
SH6G0201	SH6G0201R
SH6G1205	SH6G1205R

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SIL2 Series Mini-SIP Passive Delay Modules

- *Fast Rise Time, Low DCR*
- *High Bandwidth ≈ 0.35 / t_r*
- *Low Distortion LC Network*
- *Standard Impedances: 50 to 200 Ω*
- *Stable Delay vs. Temperature: 100 ppm/°C*
- *Operating Temperature Range -55°C to +125°C*

Electrical Specifications at 25°C [1, 2, 3, 4]

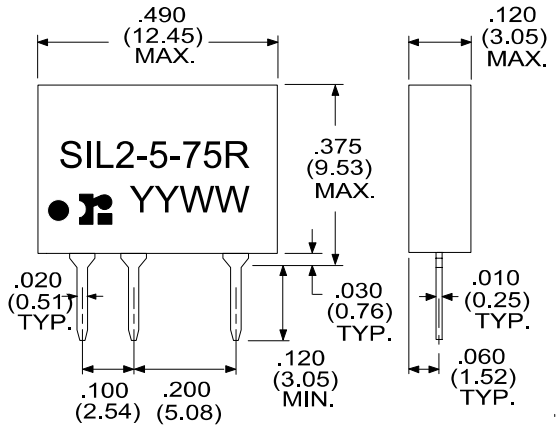
Delay (ns)	Rise Time (ns)	DCR (ohms)	50 Ohm Impedance P/N	55 Ohm Impedance P/N	75 Ohm Impedance P/N	93 Ohm Impedance P/N	100 Ohm Impedance P/N	200 Ohm Impedance P/N
0	0.1		SIL2-0	SIL2-0	SIL2-0	SIL2-0	SIL2-0	SIL2-0
1.0 ± 0.20	1.6	0.2	SIL2-1-50	SIL2-1-55	SIL2-1-75	SIL2-1-93	SIL2-1-10	SIL2-1-20
1.5 ± 0.20	1.6	0.3	SIL2-1.5-50	SIL2-1.5-55	SIL2-1.5-75	SIL2-1.5-93	SIL2-1.5-10	SIL2-1.5-20
2.0 ± 0.20	1.6	0.4	SIL2-2-50	SIL2-2-55	SIL2-2-75	SIL2-2-93	SIL2-2-10	SIL2-2-20
2.5 ± 0.20	1.6	0.5	SIL2-2.5-50	SIL2-2.5-55	SIL2-2.5-75	SIL2-2.5-93	SIL2-2.5-10	SIL2-2.5-20
3.0 ± 0.20	1.7	0.6	SIL2-3-50	SIL2-3-55	SIL2-3-75	SIL2-3-93	SIL2-3-10	SIL2-3-20
4.0 ± 0.20	1.7	0.7	SIL2-4-50	SIL2-4-55	SIL2-4-75	SIL2-4-93	SIL2-4-10	SIL2-4-20
5.0 ± 0.25	1.8	0.8	SIL2-5-50	SIL2-5-55	SIL2-5-75	SIL2-5-93	SIL2-5-10	SIL2-5-20
6.0 ± 0.30	2.0	0.85	SIL2-6-50	SIL2-6-55	SIL2-6-75	SIL2-6-93	SIL2-6-10	SIL2-6-20
7.0 ± 0.30	2.3	0.9	SIL2-7-50	SIL2-7-55	SIL2-7-75	SIL2-7-93	SIL2-7-10	SIL2-7-20
8.0 ± 0.30	2.7	0.95	SIL2-8-50	SIL2-8-55	SIL2-8-75	SIL2-8-93	SIL2-8-10	SIL2-8-20
9.0 ± 0.30	2.9	1.1	SIL2-9-50	SIL2-9-55	SIL2-9-75	SIL2-9-93	SIL2-9-10	SIL2-9-20
10.0 ± 0.30	3.3	1.2	SIL2-10-50	SIL2-10-55	SIL2-10-75	SIL2-10-93	SIL2-10-10	SIL2-10-20
11.0 ± 0.40	3.8	1.4	SIL2-11-50	SIL2-11-55	SIL2-11-75	SIL2-11-93	SIL2-11-10	SIL2-11-20
12.0 ± 0.50	4.1	1.5	SIL2-12-50	SIL2-12-55	SIL2-12-75	SIL2-12-93	SIL2-12-10	SIL2-12-20
13.0 ± 0.60	4.6	1.6	SIL2-13-50	SIL2-13-55	SIL2-13-75	SIL2-13-93	SIL2-13-10	SIL2-13-20
14.0 ± 0.70	4.9	1.6	SIL2-14-50	SIL2-14-55	SIL2-14-75	SIL2-14-93	SIL2-14-10	SIL2-14-20
15.0 ± 0.70	5.3	1.7	SIL2-15-50	SIL2-15-55	SIL2-15-75	SIL2-15-93	SIL2-15-10	SIL2-15-20
16.0 ± 0.80	5.6	1.7	SIL2-16-50	SIL2-16-55	SIL2-16-75	SIL2-16-93	SIL2-16-10	SIL2-16-20
20.0 ± 1.00	7.0	2	SIL2-20-50	SIL2-20-55	SIL2-20-75	SIL2-20-93	SIL2-20-10	SIL2-20-20

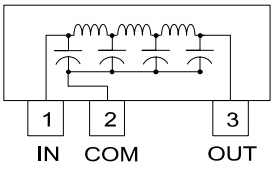
1. Rise Times are measured 20% to 80% points.
2. Delay Times measured at 50% points of leading edge.
3. Impedance, Z_O, tolerance ± 10 %
4. Output terminated to ground through $R_L = Z_O$

Operating Specifications - *Passive Delay Lines*

Pulse Overshoot (Pos) ..... 5% to 10%, typical
Pulse Distortion (S) ..... 3% typical
Working Voltage ..... 25 VDC maximum
Dielectric Strength ..... 100VDC minimum
Insulation Resistance ..... 1,000 MΩ min. @ 100VDC
Temperature Coefficient ..... 100 ppm/°C, typical
Bandwidth (f_c) ..... 0.35/t_r approx.
Operating Temperature Range ..... -55° to +125°C
Storage Temperature Range ..... -65° to +150°C

Dimensions in inches (mm)





SIL2 Series Single Output Schematic

RoHS Compliant Version

To Order RoHS Version add suffix "R":

Standard P/N	RoHS Version
SIL2-4-50	SIL2-4-50R
SIL2-15-75	SIL2-15-75R

DL22

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SL2T Series 2 Tap Mini-SIP Passive Delay Modules

- *Fast Rise Time, Low DCR*
- *High Bandwidth ≈ 0.35 / t_r*
- *Low Distortion LC Network*
- *Tap at 50% of Total Delay*
- *Standard Impedances: 50 to 200 Ω*
- *Stable Delay vs. Temperature: 100 ppm/°C*
- *Operating Temperature Range -55°C to +125°C*

Electrical Specifications at 25°C [1, 2, 3, 4]

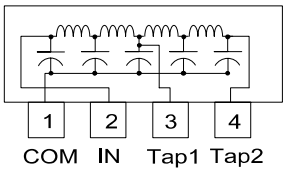
Delay (ns)	Rise Time (ns)	DCR (ohms)	50 Ohm Impedance P/N	55 Ohm Impedance P/N	75 Ohm Impedance P/N	93 Ohm Impedance P/N	100 Ohm Impedance P/N	200 Ohm Impedance P/N
0	0.1		SL2T0	SL2T0	SL2T0	SL2T0	SL2T0	SL2T0
1.0 ± 0.20	1.6	0.2	SL2T150	SL2T155	SL2T175	SL2T193	SL2T110	SL2T120
1.5 ± 0.20	1.6	0.3	SL2T1P550	SL2T1P555	SL2T1P575	SL2T1P593	SL2T1P510	SL2T1P520
2.0 ± 0.20	1.6	0.4	SL2T250	SL2T255	SL2T275	SL2T293	SL2T210	SL2T220
2.5 ± 0.20	1.6	0.5	SL2T2P550	SL2T2P555	SL2T2P575	SL2T2P593	SL2T2P510	SL2T2P520
3.0 ± 0.20	1.7	0.6	SL2T350	SL2T355	SL2T375	SL2T393	SL2T310	SL2T320
4.0 ± 0.20	1.7	0.7	SL2T450	SL2T455	SL2T475	SL2T493	SL2T410	SL2T420
5.0 ± 0.25	1.8	0.8	SL2T550	SL2T555	SL2T575	SL2T593	SL2T510	SL2T520
6.0 ± 0.30	2.0	0.85	SL2T650	SL2T655	SL2T675	SL2T693	SL2T610	SL2T620
7.0 ± 0.30	2.3	0.9	SL2T750	SL2T755	SL2T775	SL2T793	SL2T710	SL2T720
8.0 ± 0.30	2.7	0.95	SL2T850	SL2T855	SL2T875	SL2T893	SL2T810	SL2T820
9.0 ± 0.30	2.9	1.1	SL2T950	SL2T955	SL2T975	SL2T993	SL2T910	SL2T920
10.0 ± 0.30	3.3	1.2	SL2T1050	SL2T1055	SL2T1075	SL2T1093	SL2T1010	SL2T1020
11.0 ± 0.40	3.8	1.4	SL2T1150	SL2T1155	SL2T1175	SL2T1193	SL2T1110	SL2T1120
12.0 ± 0.50	4.1	1.5	SL2T1250	SL2T1255	SL2T1275	SL2T1293	SL2T1210	SL2T1220
13.0 ± 0.60	4.6	1.6	SL2T1350	SL2T1355	SL2T1375	SL2T1393	SL2T1310	SL2T1320
14.0 ± 0.70	4.9	1.6	SL2T1450	SL2T1455	SL2T1475	SL2T1493	SL2T1410	SL2T1420
15.0 ± 0.70	5.3	1.7	SL2T1550	SL2T1555	SL2T1575	SL2T1593	SL2T1510	SL2T1520
16.0 ± 0.80	5.6	1.7	SL2T1650	SL2T1655	SL2T1675	SL2T1693	SL2T1610	SL2T1620
20.0 ± 1.00	7.0	2	SL2T2050	SL2T2055	SL2T2075	SL2T2093	SL2T2010	SL2T2020

1. Rise Times are measured 20% to 80% points.
2. Delay Times measured at 50% points of leading edge
   Tap Delay = 50 % of Total
3. Impedance, Z_O, tolerance ± 10 %
4. Output terminated to ground through $R_L = Z_O$

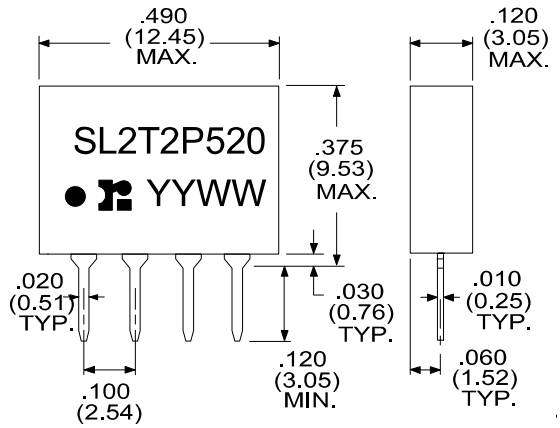
Operating Specifications - *Passive Delay Lines*

Pulse Overshoot (Pos) ..... 5% to 10%, typical
Pulse Distortion (S) ..... 3% typical
Working Voltage ..... 25 VDC maximum
Dielectric Strength ..... 100VDC minimum
Insulation Resistance ..... 1,000 MΩ min. @ 100VDC
Temperature Coefficient ..... 100 ppm/°C, typical
Bandwidth (f_C) ..... 0.35/t_r approx.
Operating Temperature Range ..... -55° to +125°C
Storage Temperature Range ..... -65° to +150°C

SL2T 2-tap Schematic



Dimensions in inches (mm)



"*SL2T*" Part Number Examples:

SL2T2P555 -- *2.5 ns (1.25ns Tap) 55 Ω*
SL2T1210 -- *12 ns (6ns Tap) 100 Ω*

RoHS Compliant Version

To Order RoHS Version add suffix "R":

Standard P/N	RoHS Version
SL2T450	SL2T450R
SL2T1575	SL2T1575R

DL22

SP3 Series 3-Pin Passive Delay Modules

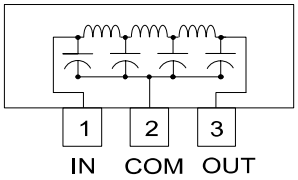
- *Fast Rise Time, Low DCR*
- *High Bandwidth ≈ 0.35 / t_r*
- *Low Distortion LC Network*
- *Standard Impedances: 50 to 200 Ω*
- *Stable Delay vs. Temperature: 100 ppm/°C*
- *Operating Temperature Range -55°C to +125°C*

Electrical Specifications at 25°C

Delay (ns)	Rise Time 20% - 80% max. (ns)	DCR max. (Ohms)	50 Ohm Impedance P/N	55 Ohm Impedance P/N	75 Ohm Impedance P/N	100 Ohm Impedance P/N	200 Ohm Impedance P/N
1 ± .20	1.6	.20	SP3-1-50	SP3-1-55	SP3-1-75	SP3-1-10	SP3-1-20
1.5 ± .20	1.6	.30	SP3-1.5-50	SP3-1.5-55	SP3-1.5-75	SP3-1.5-10	SP3-1.5-20
2 ± .20	1.6	.40	SP3-2-50	SP3-2-55	SP3-2-75	SP3-2-10	SP3-2-20
2.5 ± .20	1.6	.50	SP3-2.5-50	SP3-2.5-55	SP3-2.5-75	SP3-2.5-10	SP3-2.5-20
3 ± .20	1.7	.60	SP3-3-50	SP3-3-55	SP3-3-75	SP3-3-10	SP3-3-20
4 ± .20	1.7	.70	SP3-4-50	SP3-4-55	SP3-4-75	SP3-4-10	SP3-4-20
5 ± .25	1.8	.80	SP3-5-50	SP3-5-55	SP3-5-75	SP3-5-10	SP3-5-20
6 ± .30	2.0	.85	SP3-6-50	SP3-6-55	SP3-6-75	SP3-6-10	SP3-6-20
7 ± .30	2.3	.90	SP3-7-50	SP3-7-55	SP3-7-75	SP3-7-10	SP3-7-20
8 ± .30	2.7	.95	SP3-8-50	SP3-8-55	SP3-8-75	SP3-8-10	SP3-8-20
9 ± .30	2.9	1.10	SP3-9-50	SP3-9-55	SP3-9-75	SP3-9-10	SP3-9-20
10 ± .30	3.3	1.20	SP3-10-50	SP3-10-55	SP3-10-75	SP3-10-10	SP3-10-20
11 ± .40	3.3	1.40	SP3-11-50	SP3-11-55	SP3-11-75	SP3-11-10	SP3-11-20
12 ± .50	3.6	1.50	SP3-12-50	SP3-12-55	SP3-12-75	SP3-12-10	SP3-12-20
13 ± .60	4.0	1.60	SP3-13-50	SP3-13-55	SP3-13-75	SP3-13-10	SP3-13-20
14 ± .70	4.3	1.60	SP3-14-50	SP3-14-55	SP3-14-75	SP3-14-10	SP3-14-20
15 ± .70	4.6	1.70	SP3-15-50	SP3-15-55	SP3-15-75	SP3-15-10	SP3-15-20
16 ± .80	4.8	1.80	SP3-16-50	SP3-16-55	SP3-16-75	SP3-16-10	SP3-16-20
20 ± 1.0	5.6	2.00	SP3-20-50	SP3-20-55	SP3-20-75	SP3-20-10	SP3-20-20

1. Rise Times are measured 20% to 80% points.
2. Delay Times measured at 50% points of leading edge.
3. Impedance, Z_O, tolerance ± 10 %
4. Output terminated to ground through $R_L = Z_O$

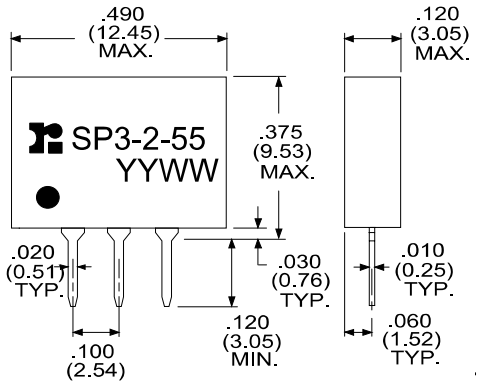
SP3 Style Schematic



Operating Specifications - *Passive Delay Lines*

Pulse Overshoot (Pos) ..... 5% to 10%, typical
Pulse Distortion (S) ..... 3% typical
Working Voltage ..... 25 VDC maximum
Dielectric Strength ..... 100VDC minimum
Insulation Resistance ..... 1,000 MΩ min. @ 100VDC
Temperature Coefficient ..... 100 ppm/°C, typical
Bandwidth (f_c) ..... 0.35/t_r approx.
Operating Temperature Range ..... -55° to +125°C
Storage Temperature Range ..... -65° to +150°C

Dimensions in inches (mm)



RoHS Compliant Version

To Order RoHS Version add suffix "R":

Standard P/N	RoHS Version
SP3-4-50	SP3-4-50R
SP3-15-75	SP3-15-75R

DL22

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SIP8 High Performance SIP Passive Delay Lines

- Fast Rise Time, Low DCR
- High Bandwidth $\approx 0.35 / t_r$
- Low Distortion LC Network
- SIngle Precise Delay Output
- Standard Impedances: 50 - 75 - 100 - 200 Ω
- Stable Delay vs. Temperature: 100 ppm/°C
- Operating Temperature Range -55°C to +125°C

Operating Specifications - *Passive Delay Lines*

Pulse Overshoot (Pos)	5% to 10%, typical
Pulse Distortion (S)	3% typical
Working Voltage	25 VDC maximum
Dielectric Strength	100VDC minimum
Insulation Resistance	1,000 MΩ min. @ 100VDC
Temperature Coefficient	100 ppm/°C, typical
Bandwidth (f_c)	0.35/t_r approx.
Operating Temperature Range	-55° to +125°C
Storage Temperature Range	-65° to +150°C

Electrical Specifications @ 25°C (1, 2, 3)

Delay (ns)	Rise Time max. (ns)	DCR max. (Ohms)	50 Ohm Impedance Part Number	75 Ohm Impedance Part Number	93 Ohm Impedance Part Number	100 Ohm Impedance Part Number	200 Ohm Impedance Part Number
1.0 ± .30	0.8	0.8	SIP8-15	SIP8-17	SIP8-19	SIP8-11	SIP8-12
1.5 ± .30	0.9	1.1	SIP8-1.55	SIP8-1.57	SIP8-1.59	SIP8-1.51	SIP8-1.52
2.0 ± .30	1.1	1.2	SIP8-25	SIP8-27	SIP8-29	SIP8-21	SIP8-22
2.5 ± .30	1.1	1.3	SIP8-2.55	SIP8-2.57	SIP8-2.59	SIP8-2.51	SIP8-2.52
3.0 ± .30	1.3	1.4	SIP8-35	SIP8-37	SIP8-39	SIP8-31	SIP8-32
4.0 ± .30	1.6	1.5	SIP8-45	SIP8-47	SIP8-49	SIP8-41	SIP8-42
5.0 ± .30	1.8	1.5	SIP8-55	SIP8-57	SIP8-59	SIP8-51	SIP8-52
6.0 ± .40	1.9	1.6	SIP8-65	SIP8-67	SIP8-69	SIP8-61	SIP8-62
7.0 ± .40	2.1	1.6	SIP8-75	SIP8-77	SIP8-79	SIP8-71	SIP8-72
8.0 ± .45	2.2	1.6	SIP8-85	SIP8-87	SIP8-89	SIP8-81	SIP8-82
9.0 ± .45	2.4	1.7	SIP8-95	SIP8-97	SIP8-99	SIP8-91	SIP8-92
10 ± .50	2.5	1.7	SIP8-105	SIP8-107	SIP8-109	SIP8-101	SIP8-102
15 ± .70	3.7	2.1	SIP8-155	SIP8-157	SIP8-159	SIP8-151	SIP8-152
20 ± 1.0	4.6	2.4	SIP8-205	SIP8-207	SIP8-209	SIP8-201	SIP8-202
25 ± 1.2	5.4	3.1	SIP8-255	SIP8-257	SIP8-259	SIP8-251	----------
30 ± 0.5	6.5	4.5	SIP8-305	SIP8-307	SIP8-309	SIP8-301	----------
50 ± 2.0	10.0	4.5	SIP8-505	SIP8-507	SIP8-509	SIP8-501	----------
100 ± 5.0	20.0	6.2	SIP8-1005	SIP8-1007	SIP8-1009	SIP8-1001	----------
200 ± 10	44.0	7.6	SIP8-2005	SIP8-2007	SIP8-2009	SIP8-2001	----------

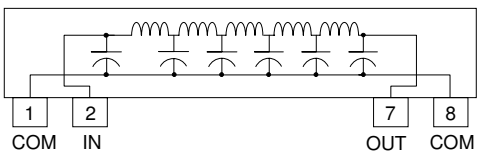
1. Rise Times are measured from 10% to 90% points.
2. Delay Times measured at 50% points of leading edge.
3. Output terminated to ground through $R_L=Z_O$

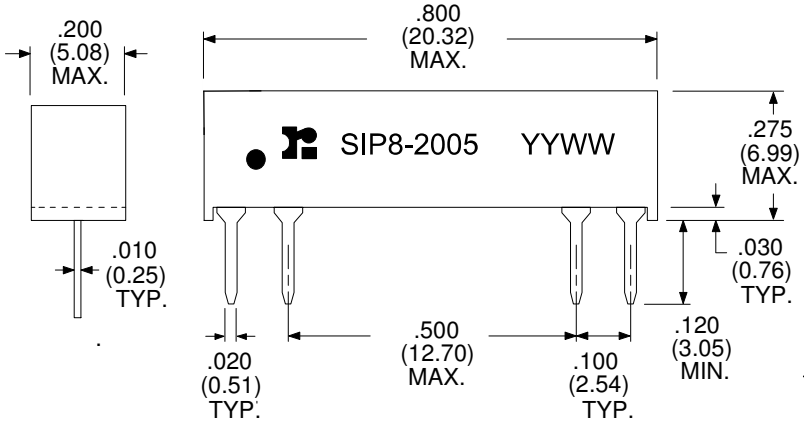
RoHS Version add suffix "R": TZB36-10R

See Similar Fixed Passives: ***"SL7T"***, ***"SL7TR"***, *& "**SH6G**" SMD*

Dimensions in inches (mm)

SIP8 Style Schematic





SL7T Series Thin SIP Passive High Performance Delay Lines

Electrical Specifications at 25°C [1, 2, 3, 4]

Delay (ns)	Rise Time 10%-90% max. (ns)	DCR max. (Ohms)	50 Ohm Impedance Part Number	75 Ohm Impedance Part Number	100 Ohm Impedance Part Number
1.0 ± .20	0.8	0.8	SL7T-15	SL7T-17	SL7T-11
1.5 ± .25	0.9	1.1	SL7T-1P55	SL7T-1P57	SL7T-1P51
2.0 ± .30	1.1	1.2	SL7T-25	SL7T-27	SL7T-21
2.5 ± .30	1.1	1.3	SL7T-2P55	SL7T-2P57	SL7T-2P51
3.0 ± .30	1.3	1.4	SL7T-35	SL7T-37	SL7T-31
3.5 ± .50	1.5	1.5	SL7T-3P55	SL7T-3P57	SL7T-3P51
4.0 ± .50	1.6	1.5	SL7T-45	SL7T-47	SL7T-41
5.0 ± .50	1.8	1.5	SL7T-55	SL7T-57	SL7T-51
6.0 ± .60	1.9	1.5	SL7T-65	SL7T-67	SL7T-61
7.0 ± .70	2.1	1.5	SL7T-75	SL7T-77	SL7T-71
7.5 ± .75	2.2	1.6	SL7T-7P55	SL7T-7P57	SL7T-7P51
8.0 ± .75	2.2	1.6	SL7T-85	SL7T-87	SL7T-81
10.0 ± .75	2.5	1.7	SL7T-105	SL7T-107	SL7T-101
12.5 ± .75	2.5	1.9	SL7T-12P55	SL7T-12P57	SL7T-12P51
15.0 ± .75	2.7	2.1	SL7T-155	SL7T-157	SL7T-151
20.0 ± 1.0	4.6	2.4	SL7T-205	SL7T-207	SL7T-201
25.0 ± 1.25	5.4	2.9	SL7T-255	SL7T-257	SL7T-251
30.0 ± 1.5	6.5	3.0	SL7T-305	SL7T-307	SL7T-301
40.0 ± 2.0	8.5	3.3	SL7T-405	SL7T-407	SL7T-401
50.0 ± 2.5	10.0	3.5	SL7T-505	SL7T-507	SL7T-501
75.0 ± 3.75	15.0	4.8	SL7T-755	SL7T-757	SL7T-751
100 ± 5.0	20.0	5.6	SL7T-1005	SL7T-1007	SL7T-1001

1. Rise Times are measured 10% to 90% points.
2. Delay Times measured at 50% points of leading edge.
3. Impedance, Z_O, tolerance ± 10 %
4. Output terminated to ground through $R_L = Z_O$

- *Fast Rise Time, Low DCR*
- *High Bandwidth* $\approx 0.35 / t_r$
- *Low Distortion LC Network*
- *SIngle Precise Delay Output*
- *Operating Temperature Range -55°C to +125°C*
- *Stable Delay vs. Temperature: 100 ppm/°C*
- *Standard Impedances: 50 - 75 - 100 Ω*
  Also Available in 200 Ω -- contact factory

Also Available in RoHS Compliant Version

Designed for use with reflow temperatures up to 245 °C max: contains high temperature solder (containing >85% lead) for internal joints exempted under RoHS Directive 2002/95/EC Annex (paragraph 7).
Lead Plating is Tin (Sn100)

For RoHS Version add "R" Suffix:

Standard P/N	RoHS Version
SL7T-1001	SL7T-1001R

OPERATING SPECIFICATIONS

Pulse Overshoot (Pos) ..... 5% to 10%, typical
Pulse Distortion (S) ..... 3% typical
Attenuation ..... 0.5 dB maximum
Working Voltage ..... 25 VDC maximum
Dielectric Strength ..... 100VDC minimum
Insulation Resistance ..... 1,000 Megohms min. @ 100VDC
Temperature Coefficient ..... 70 ppm/°C, typical
Band Width (f_C) ..... 0.35/tr approx.
Operating Temperature Range ..... -55° to +125°C
Storage Temperature Range ..... -65° to +150°C

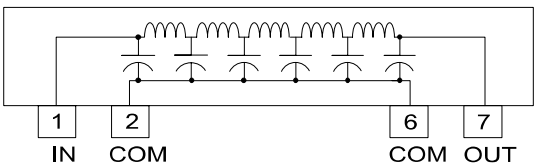
TEST CONDITIONS

(Measurements made at 25°C)
Input Rise Time ..... 2.0 ns max.
Input Pulse Period ..... 500 ns
Input Pulse Width ..... 1000 ns

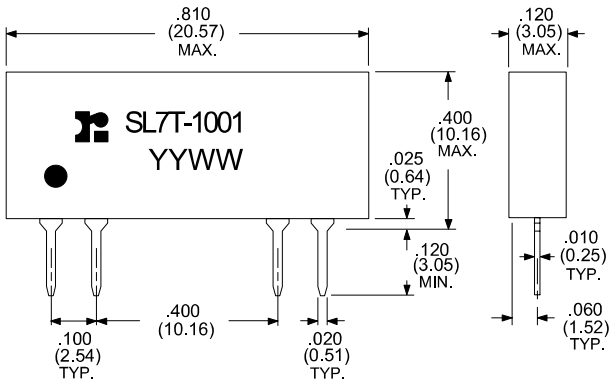
ENVIRONMENTAL

All units are designed to meet the applicable portions of MIL-D-23859, MIL-D-83531 and are capable of meeting the environmental requirements of MIL-STD-202 for moisture resistance, vibration shock, humidity and life.

SL7T Schematic Diagram



Dimensions inches (mm)



DL22

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SL7TR Series Thin SIP Passive High Performance Delay Lines

Electrical Specifications at 25°C [1, 2, 3, 4]

Delay (ns)	Rise Time 10%-90% max. (ns)	DCR max. (Ohms)	50 Ohm Impedance Part Number	75 Ohm Impedance Part Number	100 Ohm Impedance Part Number
1.0 ± .20	0.8	0.8	SL7TR-15	SL7TR-17	SL7TR-11
1.5 ± .25	0.9	1.1	SL7TR-1P55	SL7TR-1P57	SL7TR-1P51
2.0 ± .30	1.1	1.2	SL7TR-25	SL7TR-27	SL7TR-21
2.5 ± .30	1.1	1.3	SL7TR-2P55	SL7TR-2P57	SL7TR-2P51
3.0 ± .30	1.3	1.4	SL7TR-35	SL7TR-37	SL7TR-31
3.5 ± .50	1.5	1.5	SL7TR-3P55	SL7TR-3P57	SL7TR-3P51
4.0 ± .50	1.6	1.5	SL7TR-45	SL7TR-47	SL7TR-41
5.0 ± .50	1.8	1.5	SL7TR-55	SL7TR-57	SL7TR-51
6.0 ± .60	1.9	1.5	SL7TR-65	SL7TR-67	SL7TR-61
7.0 ± .70	2.1	1.5	SL7TR-75	SL7TR-77	SL7TR-71
7.5 ± .75	2.2	1.6	SL7TR-7P55	SL7TR-7P57	SL7TR-7P51
8.0 ± .75	2.2	1.6	SL7TR-85	SL7TR-87	SL7TR-81
10.0 ± .75	2.5	1.7	SL7TR-105	SL7TR-107	SL7TR-101
12.5 ± .75	2.5	1.9	SL7TR-12P55	SL7TR-12P57	SL7TR-12P51
15.0 ± .75	2.7	2.1	SL7TR-155	SL7TR-157	SL7TR-151
20.0 ± 1.0	4.6	2.4	SL7TR-205	SL7TR-207	SL7TR-201
25.0 ± 1.25	5.4	2.9	SL7TR-255	SL7T-257	SL7TR-251
30.0 ± 1.5	6.5	3.0	SL7TR-305	SL7TR-307	SL7TR-301
40.0 ± 2.0	8.5	3.3	SL7TR-405	SL7TR-407	SL7TR-401
50.0 ± 2.5	10.0	3.5	SL7TR-505	SL7TR-507	SL7TR-501
75.0 ± 3.75	15.0	4.8	SL7TR-755	SL7TR-757	SL7TR-751
100 ± 5.0	20.0	5.6	SL7TR-1005	SL7TR-1007	SL7TR-1001

1. Rise Times are measured 10% to 90% points.
2. Delay Times measured at 50% points of leading edge.
3. Impedance (Z_O) tolerance: ± 10 %
4. Output terminated to ground through $R_L = Z_O$

- *Fast Rise Time, Low DCR*
- *High Bandwidth* $\approx 0.35 / t_r$
- *Low Distortion LC Network*
- *SIngle Precise Delay Output*
- *Operating Temperature Range -55°C to +125°C*
- *Stable Delay vs. Temperature: 100 ppm/°C*
- *Standard Impedances: 50 - 75 - 100 Ω*
  Also Available in 200 Ω -- contact factory

Also Available in RoHS Compliant Version

Designed for use with reflow temperatures up to 245 °C max: contains high temperature solder (containing >85% lead) for internal joints exempted under RoHS Directive 2002/95/EC Annex (paragraph 7).
Lead Plating is Tin (Sn100)

For RoHS Version add "R" Suffix:

Standard P/N	RoHS Version
SL7TR-1001	SL7TR-1001R

OPERATING SPECIFICATIONS

Pulse Overshoot (Pos) ..... 5% to 10%, typical
Pulse Distortion (S) ..... 3% typical
Attenuation ..... 0.5 dB maximum
Working Voltage ..... 25 VDC maximum
Dielectric Strength ..... 100VDC minimum
Insulation Resistance ..... 1,000 Megohms min. @ 100VDC
Temperature Coefficient ..... 70 ppm/°C, typical
Band Width (f_c) ..... 0.35/tr approx.
Operating Temperature Range ..... -55° to +125°C
Storage Temperature Range ..... -65° to +150°C

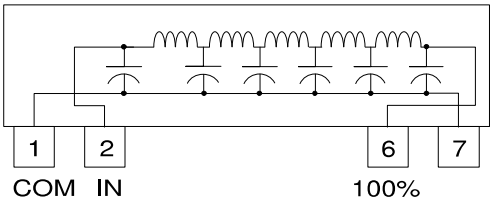
TEST CONDITIONS

(Measurements made at 25°C)
Input Rise Time ..... 2.0 ns max.
Input Pulse Period ..... 500 ns
Input Pulse Width ..... 1000 ns

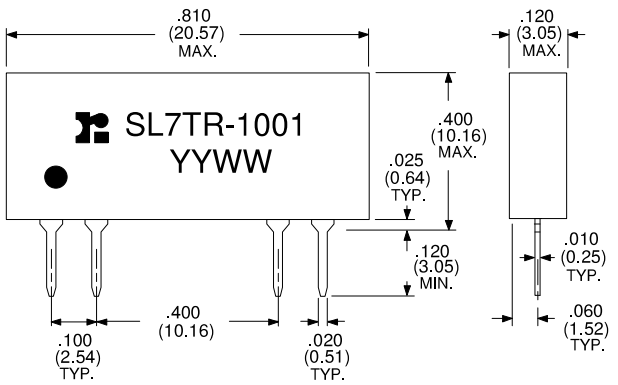
ENVIRONMENTAL

All units are designed to meet the applicable portions of MIL-D-23859, MIL-D-83531 and are capable of meeting the environmental requirements of MIL-STD-202 for moisture resistance, vibration shock, humidity and life.

SL7TR Schematic Diagram



Dimensions inches (mm)



DL22

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SIP4 Series 5-Tap High Performance Passive Delay Modules

- *Fast Rise Time, Low DCR*
- *High Bandwidth* $\approx 0.35 / t_r$
- *Low Distortion LC Network*
- *5 Equal Delay Taps*
- *Standard Impedances: 50 - 75 - 100 - 200 Ω*
- *Stable Delay vs. Temperature: 100 ppm/°C*
- *Operating Temperature Range -55°C to +125°C*

Operating Specifications - *Passive Delay Lines*

Pulse Overshoot (Pos) ..... 5% to 10%, typical
Pulse Distortion (S) ..... 3% typical
Working Voltage ..... 25 VDC maximum
Dielectric Strength ..... 100VDC minimum
Insulation Resistance ..... 1,000 MΩ min. @ 100VDC
Temperature Coefficient ..... 100 ppm/°C, typical
Bandwidth (f_c) ..... 0.35/t_r approx.
Operating Temperature Range ..... -55° to +125°C
Storage Temperature Range ..... -65° to +150°C

Low-profile DIP/SMD versions refer to **AMZ** Series !!!

Electrical Specifications at 25°C

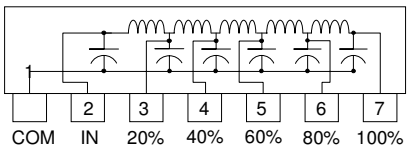
Delay Tolerances Total (ns)	Delay Tolerances Tap-to-Tap (ns)	50 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	75 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	100 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	200 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)
5 ± 0.5	1.0 ± 0.4	SIP4-55	2.0	0.7	SIP4-57	2.7	0.8	SIP4-51	3.0	0.8	SIP4-52	3.0	0.9
10 ± 1.0	2.0 ± 0.5	SIP4-105	4.0	0.7	SIP4-107	4.4	1.3	SIP4-101	4.6	1.3	SIP4-102	6.3	1.5
15 ± 1.0	3.0 ± 0.6	SIP4-155	5.5	1.0	SIP4-157	5.8	1.6	SIP4-151	5.8	1.6	SIP4-152	7.7	2.0
20 ± 1.0	4.0 ± 0.8	SIP4-205	6.4	1.2	SIP4-207	7.3	1.7	SIP4-201	7.5	1.7	SIP4-202	9.8	2.2
25 ± 1.25	5.0 ± 1.0	SIP4-255	8.0	1.3	SIP4-257	8.0	1.9	SIP4-251	8.0	1.9	SIP4-252	15.5	2.4
30 ± 1.5	6.0 ± 1.5	SIP4-305	9.0	1.6	SIP4-307	8.5	2.2	SIP4-301	8.5	2.2	SIP4-302	16.0	2.8
35 ± 1.75	7.0 ± 1.5	SIP4-355	10.0	1.7	SIP4-357	12.3	2.5	SIP4-351	12.7	2.5	SIP4-352	17.0	3.1
40 ± 2.0	8.0 ± 2.0	SIP4-405	11.0	1.9	SIP4-407	15.5	2.7	SIP4-401	15.5	2.8	SIP4-402	17.0	3.4
45 ± 2.25	9.0 ± 2.0	SIP4-455	12.0	2.0	SIP4-457	16.2	2.8	SIP4-451	16.5	3.0	SIP4-452	18.0	3.7
50 ± 2.5	10.0 ± 2.0	SIP4-505	14.0	2.1	SIP4-507	17.8	2.9	SIP4-501	18.0	3.1	SIP4-502	19.0	4.0
75 ± 3.75	15.0 ± 3.5	SIP4-755	23.0	2.2	SIP4-757	25.7	3.3	SIP4-751	26.0	3.4	–	–	–
100 ± 5.0	20.0 ± 4.0	SIP4-1005	33.0	2.4	SIP4-1007	34.0	3.6	SIP4-1001	34.0	3.7	–	–	–

1. Rise Times are measured from 10% to 90% points.
2. Delay Times measured at 50% points of leading edge.
3. Output (100% Tap) terminated to ground through $R_L=Z_O$

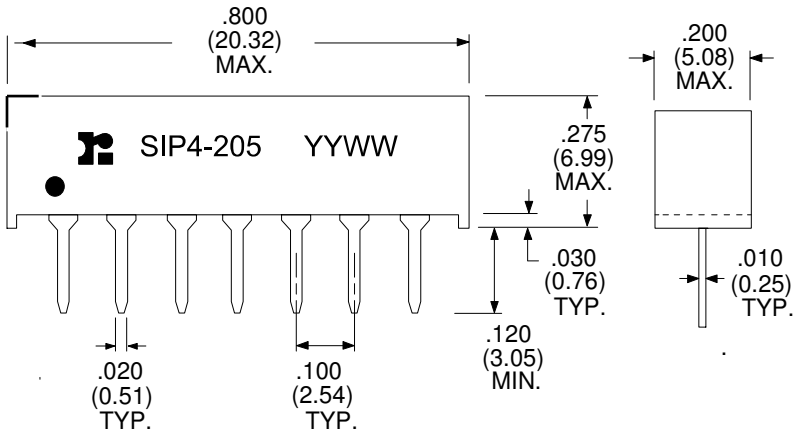
*See Similar 5 Tap Passives: "**AMZ**" DIP/SMD, "**TZA**"*

RoHS Version add suffix "R": SIP4-507R

5-Tap SIP4 Style Schematic



Dimensions in inches (mm)



SIP5 Series 10-Tap High Performance Passive Delays

- *Fast Rise Time, Low DCR*
- *High Bandwidth* $\approx 0.35 / t_r$
- *Low Distortion LC Network*
- *10 Equal Delay Taps*
- *Standard Impedances: 50 - 75 - 100 - 200 Ω*
- *Stable Delay vs. Temperature: 100 ppm/°C*
- *Operating Temperature Range -55°C to +125°C*

Operating Specifications - *Passive Delay Lines*

Pulse Overshoot (Pos) ..... 5% to 10%, typical
Pulse Distortion (S) ..... 3% typical
Working Voltage ..... 25 VDC maximum
Dielectric Strength ..... 100VDC minimum
Insulation Resistance ..... 1,000 MΩ min. @ 100VDC
Temperature Coefficient ..... 100 ppm/°C, typical
Bandwidth (f_c) ..... 0.35/t_r approx.
Operating Temperature Range ..... -55° to +125°C
Storage Temperature Range ..... -65° to +150°C

Electrical Specifications at 25°C

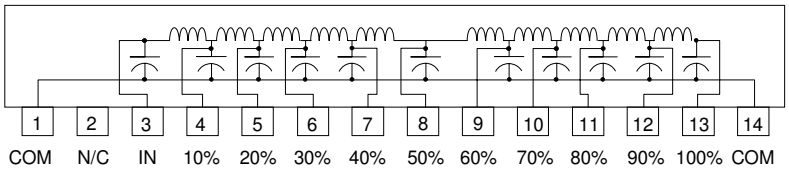
Delay Tolerances Total (ns)	Delay Tolerances Tap-to-Tap (ns)	50 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	75 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	100 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	200 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)
5 ± 0.5	0.5 ± 0.2	SIP5-55	2.0	0.7	SIP5-57	2.1	0.8	SIP5-51	2.2	0.8	SIP5-52	2.4	0.9
10 ± 0.7	1.0 ± 0.4	SIP5-105	3.2	0.7	SIP5-107	3.6	0.8	SIP5-101	3.8	0.8	SIP5-102	5.5	1.0
15 ± 1.0	1.5 ± 0.5	SIP5-155	3.4	0.8	SIP5-157	4.1	1.2	SIP5-151	4.1	1.3	SIP5-152	6.3	1.5
20 ± 1.0	2.0 ± 0.5	SIP5-205	4.0	0.8	SIP5-207	4.4	1.3	SIP5-201	4.6	1.5	SIP5-202	8.5	1.5
25 ± 1.25	2.5 ± 0.5	SIP5-255	4.5	0.9	SIP5-257	5.3	1.5	SIP5-251	5.5	1.7	SIP5-252	9.0	2.2
30 ± 1.5	3.0 ± 0.6	SIP5-305	5.5	1.0	SIP5-307	5.8	1.7	SIP5-301	5.8	2.0	SIP5-302	10.0	2.4
35 ± 1.75	3.5 ± 0.8	SIP5-355	6.6	1.2	SIP5-357	7.2	2.0	SIP5-351	7.3	2.2	SIP5-352	13.0	2.5
40 ± 2.0	4.0 ± 1.0	SIP5-405	7.0	1.2	SIP5-407	7.5	2.0	SIP5-401	7.5	2.2	SIP5-402	13.4	3.0
45 ± 2.25	4.5 ± 1.0	SIP5-455	8.2	1.3	SIP5-457	8.2	2.1	SIP5-451	8.3	2.3	SIP5-452	15.2	3.1
50 ± 2.5	5.0 ± 1.0	SIP5-505	8.5	1.3	SIP5-507	8.5	2.1	SIP5-501	8.5	2.3	SIP5-502	15.5	3.3
55 ± 2.75	5.5 ± 1.0	SIP5-555	10.2	1.6	SIP5-557	11.2	2.2	SIP5-551	11.4	2.4	SIP5-552	16.0	3.5
60 ± 3.0	6.0 ± 1.5	SIP5-605	10.5	1.6	SIP5-607	11.4	2.3	SIP5-601	11.5	2.5	SIP5-602	16.2	3.6
70 ± 3.5	7.0 ± 1.5	SIP5-705	11.0	1.7	SIP5-707	13.0	2.6	SIP5-701	13.0	2.8	SIP5-702	17.0	3.7
75 ± 3.75	7.5 ± 1.5	SIP5-755	11.6	1.9	SIP5-757	15.0	2.8	SIP5-751	15.3	3.0	SIP5-752	19.1	3.8
80 ± 4.0	8.0 ± 1.8	SIP5-805	12.0	1.9	SIP5-807	15.3	2.9	SIP5-801	15.5	3.0	SIP5-802	19.5	4.0
90 ± 4.5	9.0 ± 2.0	SIP5-905	14.0	2.0	SIP5-907	17.3	3.0	SIP5-901	17.5	3.1	SIP5-902	20.0	4.2
100 ± 5.0	10.0 ± 2.0	SIP5-1005	18.0	2.1	SIP5-1007	19.5	3.1	SIP5-1001	20.0	3.2	SIP5-1002	24.0	4.4

1. Rise Times are measured from 10% to 90% points.
2. Delay Times measured at 50% points of leading edge.
3. Output (100% Tap) terminated to ground through $R_L=Z_O$

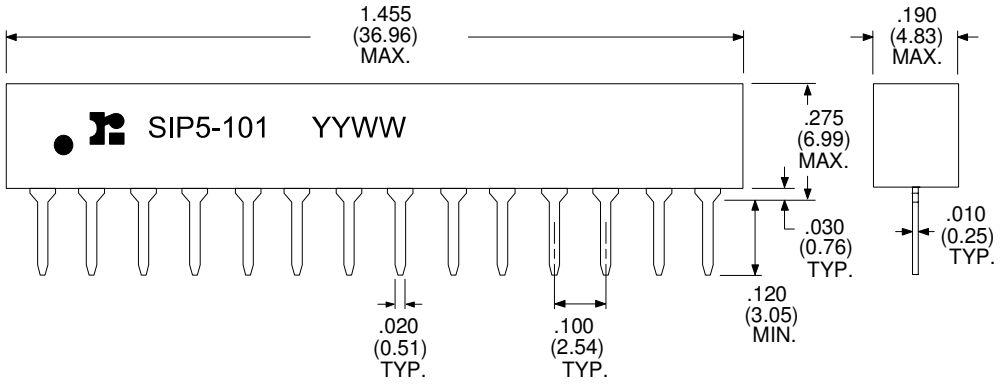
RoHS Version add suffix "R": SIP5-302R

*See Similar 10 Tap Passives: "**AIZ**" DIP/SMD, "**TZB**" & "**TF**"*

10-Tap *SIP5* Style Schematic



Dimensions in inches (mm)



DL22

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TZA / TYA Series 5-Tap High Performance Passive Delay Modules

- *Fast Rise Time, Low DCR*
- *High Bandwidth $\approx$ 0.35 / t_r*
- *Low Distortion LC Network*
- *5 Equal Delay Taps*
- *Standard Impedances: 50 - 75 - 100 - 200 Ω*
- *Stable Delay vs. Temperature: 100 ppm/°C*
- *Operating Temperature Range -55°C to +125°C*

Operating Specifications - *Passive Delay Lines*

Pulse Overshoot (Pos) ..... 5% to 10%, typical
Pulse Distortion (S) ..... 3% typical
Working Voltage ..... 25 VDC maximum
Dielectric Strength ..... 100VDC minimum
Insulation Resistance ..... 1,000 MΩ min. @ 100VDC
Temperature Coefficient ..... 100 ppm/°C, typical
Bandwidth (f_c) ..... 0.35/t_r approx.
Operating Temperature Range ..... -55° to +125°C
Storage Temperature Range ..... -65° to +150°C

Low-profile DIP/SMD versions refer to **AMZ** Series

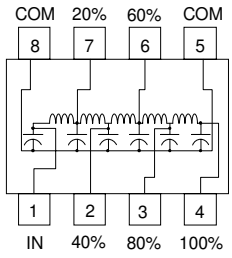
Electrical Specifications at 25°C

Delay Tolerances Total (ns)	Delay Tolerances Tap-to-Tap (ns)	50 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	75 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	100 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	200 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)
5 ± 0.5	1.0 ± 0.4	TZA1-5	2.0	0.7	TZA1-7	2.7	0.8	TZA1-10	3.0	0.8	TZA1-20	3.0	0.9
10 ± 1.0	2.0 ± 0.5	TZA2-5	4.0	0.7	TZA2-7	4.4	1.3	TZA2-10	4.6	1.3	TZA2-20	6.3	1.5
15 ± 1.0	3.0 ± 0.6	TZA3-5	5.5	1.0	TZA3-7	5.8	1.6	TZA3-10	5.8	1.6	TZA3-20	7.7	2.0
20 ± 1.0	4.0 ± 0.8	TZA4-5	6.4	1.2	TZA4-7	7.3	1.7	TZA4-10	7.5	1.7	TZA4-20	9.8	2.2
25 ± 1.25	5.0 ± 1.0	TZA5-5	8.0	1.3	TZA5-7	8.0	1.9	TZA5-10	8.0	1.9	TZA5-20	15.5	2.4
30 ± 1.5	6.0 ± 1.2	TZA6-5	9.0	1.6	TZA6-7	8.5	2.2	TZA6-10	8.5	2.2	TZA6-20	16.0	2.8
35 ± 1.75	7.0 ± 1.5	TZA7-5	10.0	1.7	TZA7-7	12.3	2.5	TZA7-10	12.7	2.5	TZA7-20	17.0	3.1
40 ± 2.0	8.0 ± 2.0	TZA8-5	11.0	1.9	TZA8-7	15.5	2.8	TZA8-10	15.5	2.8	TZA8-20	17.0	3.4
45 ± 2.25	9.0 ± 2.0	TZA9-5	12.0	2.0	TZA9-7	16.2	3.0	TZA9-10	16.5	3.0	TZA9-20	18.0	3.7
50 ± 2.5	10.0 ± 2.0	TZA10-5	14.0	2.1	TZA10-7	17.8	3.1	TZA10-10	18.0	3.1	TZA10-20	19.0	4.0
75 ± 3.75	15.0 ± 3.5	TZA11-5	23.0	2.2	TZA11-7	25.7	3.4	TZA11-10	26.0	3.4	–	–	–
100 ± 5.0	20.0 ± 4.0	TZA12-5	33.0	2.4	TZA12-7	34.0	3.7	TZA12-10	34.0	3.7	–	–	–
125 ± 6.25	25.0 ± 5.0	TZA13-5	35.0	2.6	TZA13-7	41.5	4.0	TZA13-10	42.0	4.0	–	–	–

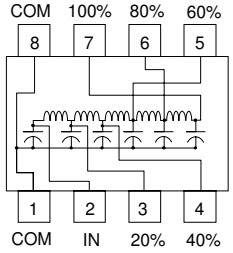
1. Rise Times are measured from 10% to 90% points.
2. Delay Times measured at 50% points of leading edge.
3. Output (100% Tap) terminated to ground through $R_L=Z_O$

RoHS Version add suffix "R": TZA4-5R

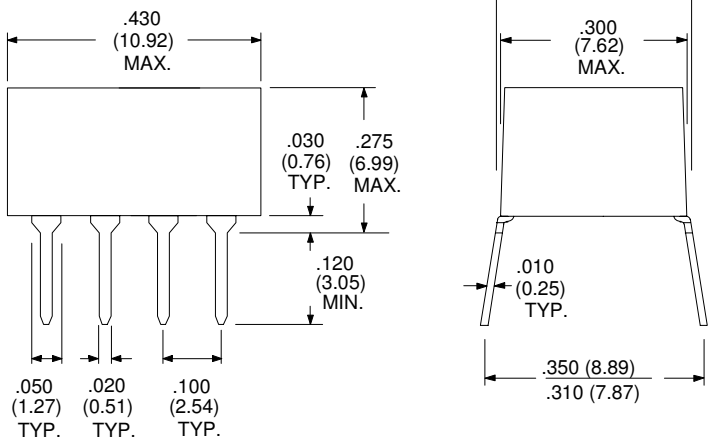
TZA Style Schematic
Most Popular Footprint



TYA Style Schematic
Substitute TYA for TZA in P/N



Dimensions
in inches (mm)



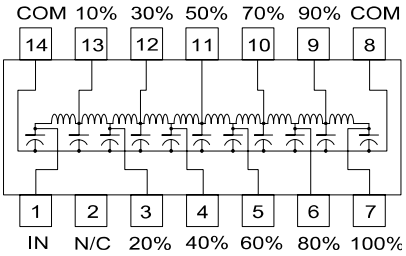
TZB-TYB-TUB Series 10-Tap High Performance Passive Delays

- *Fast Rise Time, Low DCR*
- *High Bandwidth* $\approx 0.35 / t_r$
- *Low Distortion LC Network*
- *10 Equal Delay Taps*
- *Standard Impedances: 50 - 75 - 100 - 200 Ω*
- *Stable Delay vs. Temperature: 100 ppm/°C*
- *Operating Temperature Range -55°C to +125°C*

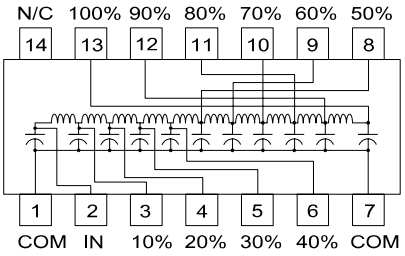
Operating Specifications - *Passive Delay Lines*

Pulse Overshoot (Pos)	5% to 10%, typical
Pulse Distortion (S)	3% typical
Working Voltage	25 VDC maximum
Dielectric Strength	100VDC minimum
Insulation Resistance	1,000 MΩ min. @ 100VDC
Temperature Coefficient	100 ppm/°C, typical
Bandwidth (f_C)	0.35/t_r approx.
Operating Temperature Range	-55° to +125°C
Storage Temperature Range	-65° to +150°C

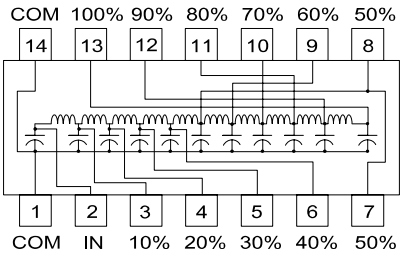
TZB Style Schematic
Most Popular Footprint



TYB Style Schematic
Substitute TYB for TZB in P/N



TUB Style Schematic
Substitute TUB for TZB in P/N



Electrical Specifications at 25°C

*Low-profile DIP/SMD versions refer to **AIZ** Series*

Delay Tolerances Total (ns)	Delay Tolerances Tap-to-Tap (ns)	50 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	75 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	100 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	200 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)
5 ± 0.5	0.5 ± 0.2	TZB1-5	2.0	0.7	TZB1-7	2.1	0.8	TZB1-10	2.2	0.8	TZB1-20	2.4	0.9
10 ± 0.7	1.0 ± 0.4	TZB6-5	3.2	0.7	TZB6-7	3.6	0.8	TZB6-10	3.8	0.8	TZB6-20	5.5	1.0
20 ± 1.0	2.0 ± 0.5	TZB12-5	4.0	0.7	TZB12-7	4.4	1.3	TZB12-10	4.6	1.5	TZB12-20	8.5	1.5
25 ± 1.25	2.5 ± 0.5	TZB18-5	4.5	0.9	TZB18-7	5.3	1.5	TZB18-10	5.5	1.7	TZB18-20	9.0	1.8
30 ± 1.5	3.0 ± 0.5	TZB24-5	5.5	1.0	TZB24-7	5.8	1.7	TZB24-10	5.8	2.0	TZB24-20	10.0	2.0
40 ± 2.0	4.0 ± 1.0	TZB30-5	7.0	1.2	TZB30-7	7.5	2.0	TZB30-10	7.5	2.2	TZB30-20	13.0	2.2
50 ± 2.5	5.0 ± 1.0	TZB36-5	8.5	1.3	TZB36-7	8.5	2.1	TZB36-10	8.5	2.3	TZB36-20	15.5	2.4
60 ± 3.0	6.0 ± 1.5	TZB42-5	10.5	1.6	TZB42-7	11.4	2.3	TZB42-10	11.5	2.5	TZB42-20	16.0	2.5
70 ± 3.5	7.0 ± 1.5	TZB48-5	11.0	1.7	TZB48-7	13.0	2.5	TZB48-10	13.0	2.8	TZB48-20	17.0	2.5
80 ± 4.0	8.0 ± 1.8	TZB54-5	12.0	1.9	TZB54-7	15.3	3.8	TZB54-10	15.5	3.0	TZB54-20	19.0	2.5
90 ± 4.5	9.0 ± 2.0	TZB60-5	14.0	2.0	TZB60-7	17.3	3.0	TZB60-10	17.5	3.1	TZB60-20	20.0	2.5
100 ± 5.0	10.0 ± 2.0	TZB66-5	18.0	2.1	TZB66-7	19.5	3.1	TZB66-10	20.0	3.2	TZB66-20	24.0	2.5
150 ± 7.50	15.0 ± 3.0	TZB72-5	24.0	2.2	TZB72-7	26.0	3.3	TZB72-10	26.0	3.5	TZB72-20	35.0	3.6
200 ± 10.0	20.0 ± 3.0	TZB78-5	34.0	2.4	TZB78-7	38.0	3.4	TZB78-10	39.0	3.5	TZB78-20	44.0	4.8
250 ± 12.5	25.0 ± 3.0	TZB84-5	41.0	2.4	TZB84-7	45.0	3.5	TZB84-10	46.0	4.0	TZB84-20	56.0	5.2
300 ± 15.0	30.0 ± 3.0	TZB90-5	48.0	2.5	TZB90-7	53.0	3.5	TZB90-10	54.0	4.2	TZB90-20	68.0	5.8
400 ± 20.0	40.0 ± 5.0	TZB94-5	65.0	2.8	TZB94-7	66.0	3.6	TZB94-10	67.0	4.5	-----	-----	-----
500 ± 25.0	50.0 ± 5.0	TZB98-5	75.0	3.3	TZB98-7	84.0	3.7	TZB98-10	86.0	5.0	-----	-----	-----

1. Rise Times are measured from 10% to 90% points.
2. Delay Times measured at 50% points of leading edge.
3. Output (100% Tap) terminated to ground through $R_L=Z_O$

P/N Description

TZB* XX - *XX

Passive 10 Tap Thru-hole
14-pin Delay Module Series

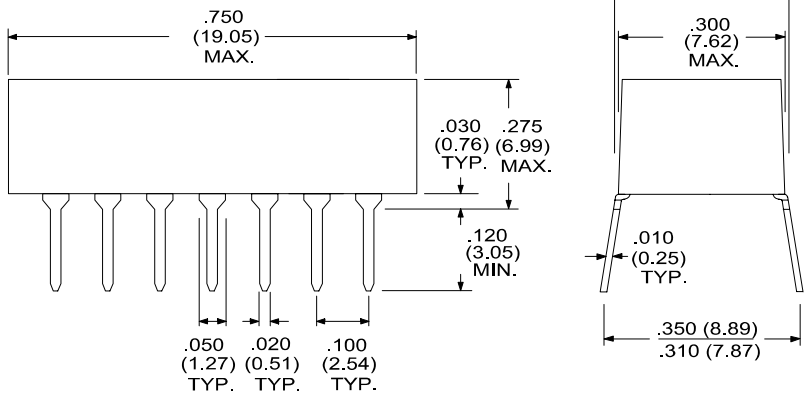
Delay Coding Number
Per Table above

Impedance Specifier:
50 Ohms = 5
75 Ohms = 7
100 Ohms = 10
200 Ohms = 20

RoHS Version add suffix "R": TZB36-10R

Part Number Examples:
TZB6-10 = 10 ns, 1 ns / tap , 100 Ω, 14-pin
TZB18-7R = 25 ns, 2.5 ns / tap , 75 Ω, 14-pin RoHS
TZB98-5 = 500 ns, 50 ns / tap , 50 Ω, 14-pin

Dimensions in inches (mm)



DL22

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TF Series Fast Rise Time High Performance 20 Section 10-Tap Passive 28-Pin Delay Lines

- *Fast Rise Time (t_d / t_r 10)*
- *High Bandwidth 0.35 / t_r*
- *Low Distortion LC Network*
- *10 Equal Delay Taps*
- *Standard Impedances: 50 - 75 - 100 - 200 Ω*
- *Stable Delay vs. Temperature: 100 ppm/°C*
- *Operating Temperature Range -55°C to +125°C*

Operating Specifications - *Passive Delay Lines*

Pulse Overshoot (Pos)	5% to 10%, typical
Pulse Distortion (S)	3% typical
Working Voltage	25 VDC maximum
Dielectric Strength	100VDC minimum
Insulation Resistance	1,000 MΩ min. @ 100VDC
Temperature Coefficient	100 ppm/°C, typical
Bandwidth (f_c)	0.35/t_r approx.
Operating Temperature Range	-55° to +125°C
Storage Temperature Range	-65° to +150°C

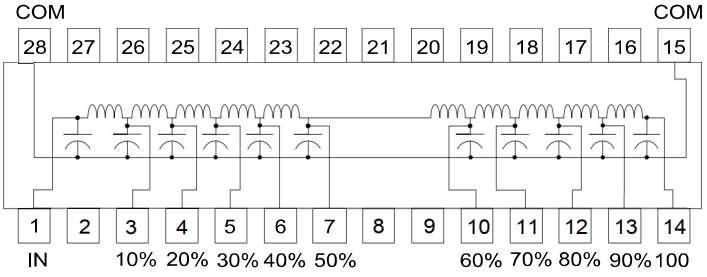
Electrical Specifications at 25°C [1, 2, 3]

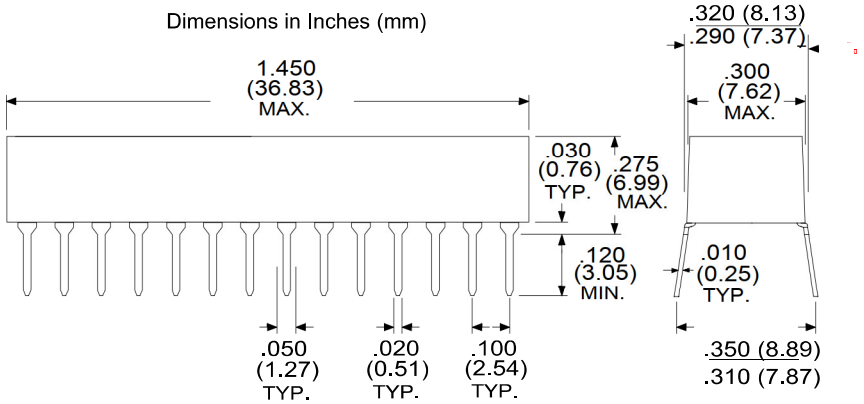
Delay Tolerances Total (ns)	Delay Tolerances Tap-to-Tap (ns)	50 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	75 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	100 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)
50 ± 2.5	5.0 ± 1.0	TF50-5	6.2	1.9	TF50-7	6.2	2.0	TF50-10	6.4	2.2
75 ± 3.7	7.5 ± 2.0	TF75-5	9.2	2.1	TF75-7	9.2	2.2	TF75-10	9.4	2.3
80 ± 4.0	8.0 ± 2.0	TF80-5	9.5	2.2	TF80-7	9.6	2.3	TF80-10	9.9	2.4
100 ± 5.0	10.0 ± 2.0	TF100-5	11.2	2.3	TF100-7	11.7	2.5	TF100-10	12.5	2.7
120 ± 6.0	12.0 ± 2.0	TF120-5	13.4	2.3	TF120-7	13.7	2.7	TF120-10	13.8	3.1
150 ± 15.0	15.0 ± 2.5	TF150-5	15.7	2.4	TF150-7	16.1	3.1	TF150-10	16.4	3.5
200 ± 10.0	20.0 ± 3.0	TF200-5	21.3	2.5	TF200-7	21.5	3.3	TF200-10	21.6	3.8
250 ± 12.5	25.0 ± 3.0	TF250-5	27.2	2.6	TF250-7	27.3	3.5	TF250-10	27.5	4.3
300 ± 15.0	30.0 ± 3.5	TF300-5	31.1	2.7	TF300-7	31.4	3.6	TF300-10	32.3	4.6
400 ± 20.0	40.0 ± 4.0	TF400-5	41.0	2.8	TF400-7	41.3	3.7	TF400-10	41.7	4.8
500 ± 25.0	50.0 ± 5.0	TF500-5	50.8	2.9	TF500-7	53.1	3.9	TF500-10	54.2	5.1

1. Rise Times are measured from 10% to 90% points.
2. Delay Times measured at 50% points of leading edge.
3. Output (100% Tap) terminated through Z_o to ground.

RoHS Version add suffix "R": TF300-5R

TF Schematic Diagram





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SP24A Series 20-Tap High Performance Passive Delay Modules

- *Fast Rise Time, Low DCR*
- *High Bandwidth* $\approx 0.35 / t_r$
- *Low Distortion LC Network*
- *20 Equal Delay Taps*
- *Standard Impedances: 50 - 75 - 100 - 200 Ω*
- *Stable Delay vs. Temperature: 100 ppm/°C*
- *Operating Temperature Range -55°C to +125°C*

Operating Specifications - *Passive Delay Lines*

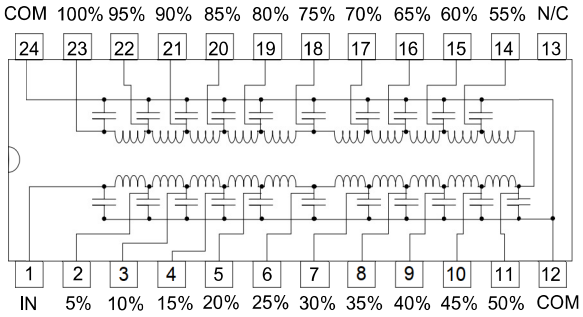
Pulse Overshoot (Pos)	5% to 10%, typical
Pulse Distortion (S)	3% typical
Working Voltage	25 VDC maximum
Dielectric Strength	100VDC minimum
Insulation Resistance	1,000 MΩ min. @ 100VDC
Temperature Coefficient	70 ppm/°C, typical
Bandwidth (f_C)	0.35/t_r approx.
Operating Temperature Range	-55° to +125°C
Storage Temperature Range	-65° to +150°C

Electrical Specifications [1, 2, 3] at 25°C *Note: For SMD Package Add "G" to end of P/N in Table Below*

Total (ns)	Tap-to-Tap (ns)	50 Ohm Part Number	Rise Time max. (ns)	DCR max. (Ohms)	75 Ohm Part Number	Rise Time max. (ns)	DCR max. (Ohms)	100 Ohm Part Number	Rise Time max. (ns)	DCR max. (Ohms)	200 Ohm Part Number	Rise Time max. (ns)	DCR max. (Ohms)
10 ± 0.50	0.5 ± 0.2	SP24A-105	2.5	1.0	SP24A-107	2.5	1.0	SP24A-101	2.8	1.3	SP24A-102	3.5	2.5
20 ± 1.00	1.0 ± 0.4	SP24A-205	3.7	1.7	SP24A-207	3.7	1.7	SP24A-201	3.7	1.8	SP24A-202	4.0	3.9
25 ± 1.25	1.25 ± 0.5	SP24A-255	4.0	1.8	SP24A-257	4.0	1.8	SP24A-251	4.0	2.1	SP24A-252	4.5	4.4
30 ± 1.50	1.5 ± 0.5	SP24A-305	4.8	1.9	SP24A-307	4.8	1.9	SP24A-301	4.8	2.3	SP24A-302	5.0	4.8
40 ± 2.00	2.0 ± 0.5	SP24A-405	5.5	2.1	SP24A-407	5.5	2.1	SP24A-401	5.5	2.4	SP24A-402	7.5	5.0
50 ± 2.50	2.5 ± 0.5	SP24A-505	6.0	2.2	SP24A-507	6.0	2.2	SP24A-501	6.2	2.6	SP24A-502	9.0	5.2
60 ± 3.00	3.0 ± 0.6	SP24A-605	7.0	2.4	SP24A-607	7.0	2.4	SP24A-601	7.1	2.7	SP24A-602	10.0	5.3
70 ± 3.50	3.5 ± 0.8	SP24A-705	7.9	2.6	SP24A-707	7.9	2.6	SP24A-701	8.1	2.8	SP24A-702	11.0	5.4
75 ± 3.75	3.75 ± 0.8	SP24A-755	8.7	2.6	SP24A-757	8.8	2.6	SP24A-751	8.8	2.9	SP24A-752	11.5	5.5
80 ± 4.00	4.0 ± 1.0	SP24A-805	9.4	2.8	SP24A-807	9.4	2.8	SP24A-801	9.5	3.0	SP24A-802	12.0	5.7
100 ± 5.00	5.0 ± 1.0	SP24A1005	11.8	3.0	SP24A1007	11.9	3.3	SP24A1001	11.9	3.3	SP24A1002	15.0	6.0
150 ± 7.50	7.5 ± 2.0	SP24A1505	15.5	3.4	SP24A1507	16.0	3.7	SP24A1501	16.0	3.7	SP24A1502	23.0	7.0
200 ± 10.0	10.0 ± 2.0	SP24A2005	20.0	3.6	SP24A2007	18.9	4.1	SP24A2001	18.9	4.1	SP24A2002	31.0	8.1
250 ± 12.5	12.5 ± 3.0	SP24A2505	26.0	3.8	SP24A2507	24.5	4.2	SP24A2501	24.5	4.3	SP24A2502	38.0	9.2
300 ± 15.0	15.0 ± 3.0	SP24A3005	32.0	4.4	SP24A3007	29.0	4.5	SP24A3001	29.0	4.8	SP24A3002	46.0	9.9
400 ± 20.0	20.0 ± 4.0	SP24A4005	38.0	4.5	SP24A4007	38.0	4.7	SP24A4001	38.0	4.9	---	---	---
500 ± 25.0	25.0 ± 5.0	SP24A5005	46.0	4.8	SP24A5007	46.0	4.9	SP24A5001	46.0	5.2	---	---	---

1. Rise Times are measured from 10% to 90% points.
2. Delay Times measured at 50% points of leading edge.
3. Output (100% Tap) terminated to ground through $R_L = Z_O$

SP24A Style 20-Tap Schematic

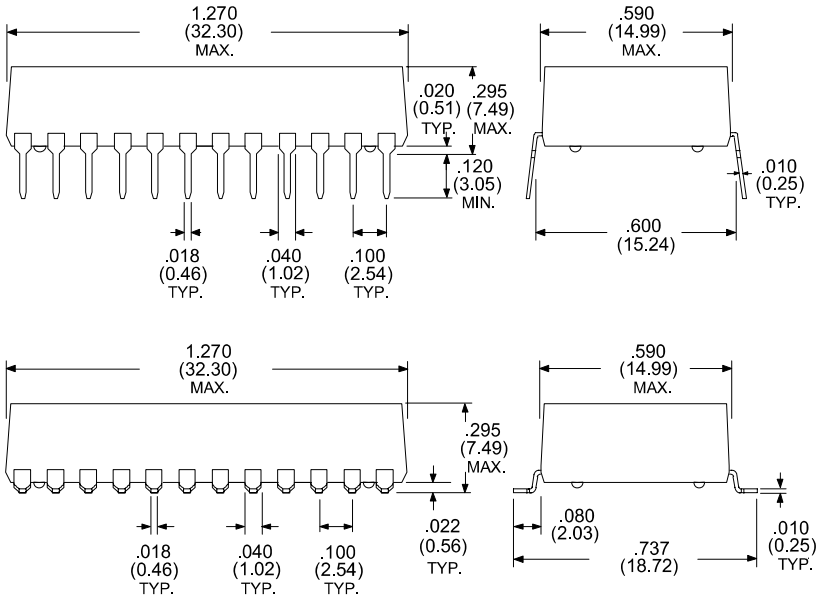


Alternate Pinout, Similar 20 Tap Electricals, refer to Series ***SP24***

Also, for same 24-Pin package and Single Output refer to Series ***SP24L***

Dimensions in Inches (mm)

Default Thru-hole 24-Pin Package. Example: SP24A-105



Gull wing SMD Package Add suffix "G" to P/N. Example: SP24A-105G

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SP24 Series 20-Tap High Performance Passive Delay Modules

- *Fast Rise Time, Low DCR*
- *High Bandwidth* $\approx 0.35 / t_r$
- *Low Distortion LC Network*
- *20 Equal Delay Taps*
- *Standard Impedances: 50 - 75 - 100 - 200 Ω*
- *Stable Delay vs. Temperature: 100 ppm/°C*
- *Operating Temperature Range -55°C to +125°C*

Operating Specifications - *Passive Delay Lines*

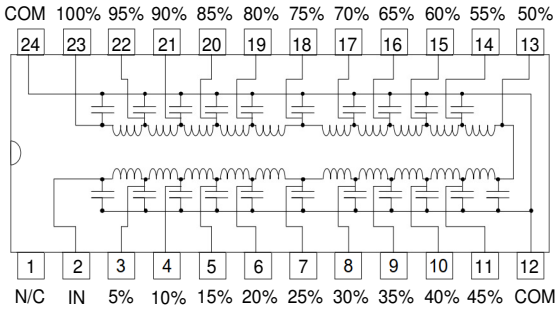
Pulse Overshoot (Pos)	5% to 10%, typical
Pulse Distortion (S)	3% typical
Working Voltage	25 VDC maximum
Dielectric Strength	100VDC minimum
Insulation Resistance	1,000 MΩ min. @ 100VDC
Temperature Coefficient	70 ppm/°C, typical
Bandwidth (f_C)	0.35/t_r approx.
Operating Temperature Range	-55° to +125°C
Storage Temperature Range	-65° to +150°C

Electrical Specifications [1, 2, 3] at 25°C *Note: For SMD Package Add "G" to end of P/N in Table Below*

Total Delay (ns)	Tap-to-Tap Delay (ns)	50 Ohm Impedance P/N	Rise Time max. (ns)	DCR (ohms)	75 Ohm Impedance P/N	Rise Time max. (ns)	DCR (ohms)	100 Ohm Impedance P/N	Rise Time max. (ns)	DCR (ohms)	200 Ohm Impedance P/N	Rise Time max. (ns)	DCR (ohms)
10 ± 0.5	0.5 ± 0.2	SP24-105	2.5	1.0	SP24-107	2.5	1.0	SP24-101	2.8	1.3	SP24-102	3.5	2.5
20 ± 1.00	1.0 ± 0.4	SP24-205	3.7	1.7	SP24-207	3.7	1.7	SP24-201	3.7	1.8	SP24-202	4.0	3.9
25 ± 1.25	1.3 ± 0.5	SP24-255	4.0	1.8	SP24-257	4.0	1.8	SP24-251	4.0	2.1	SP24-252	4.5	4.4
30 ± 1.50	1.5 ± 0.5	SP24-305	4.8	1.9	SP24-307	4.8	1.9	SP24-301	4.8	2.3	SP24-302	5.0	4.8
40 ± 2.00	2.0 ± 0.5	SP24-405	5.5	2.1	SP24-407	5.5	2.1	SP24-401	5.5	2.4	SP24-402	7.5	5.0
50 ± 2.50	2.5 ± 0.5	SP24-505	6.0	2.2	SP24-507	6.0	2.2	SP24-501	6.2	2.6	SP24-502	9.0	5.2
60 ± 3.00	3.0 ± 0.6	SP24-605	7.0	2.4	SP24-607	7.0	2.4	SP24-601	7.1	2.7	SP24-602	10.0	5.3
70 ± 3.50	3.5 ± 0.8	SP24-705	7.9	2.6	SP24-707	7.9	2.6	SP24-701	8.1	2.8	SP24-702	11.0	5.4
75 ± 3.75	3.8 ± 0.8	SP24-755	8.7	2.6	SP24-757	8.8	2.6	SP24-751	8.8	2.9	SP24-752	11.5	5.5
80 ± 4.00	4.0 ± 1.0	SP24-805	9.4	2.8	SP24-807	9.4	2.8	SP24-801	9.5	3.0	SP24-802	12.0	5.7
100 ± 5.00	5.0 ± 1.0	SP24-1005	11.8	3.0	SP24-1007	11.9	3.3	SP24-1001	11.9	3.3	SP24-1002	15.0	6.0
150 ± 7.50	7.5 ± 2.0	SP24-1505	15.5	3.4	SP24-1507	16.0	3.7	SP24-1501	16.0	3.7	SP24-1502	23.0	7.0
200 ± 10.00	10.0 ± 2.0	SP24-2005	20.0	3.6	SP24-2007	18.9	4.1	SP24-2001	18.9	4.1	SP24-2002	31.0	8.1
250 ± 12.50	12.5 ± 3.0	SP24-2505	26.0	3.8	SP24-2507	24.5	4.2	SP24-2501	24.5	4.3	SP24-2502	38.0	9.2
300 ± 15.00	15.0 ± 3.0	SP24-3005	32.0	4.4	SP24-3007	29.0	4.5	SP24-3001	29.0	4.8	SP24-3002	46.0	9.9
400 ± 20.00	20.0 ± 4.0	SP24-4005	38.0	4.5	SP24-4007	38.0	4.7	SP24-4001	38.0	4.9	----	----	----
500 ± 25.00	25.0 ± 5.0	SP24-5005	46.0	4.8	SP24-5007	46.0	4.9	SP24-5001	46.0	5.2	----	----	----

1. Rise Times are measured from 10% to 90% points.
2. Delay Times measured at 50% points of leading edge.
3. Output (100% Tap) terminated to ground through $R_L=Z_O$

SP24 Style 20-Tap Schematic

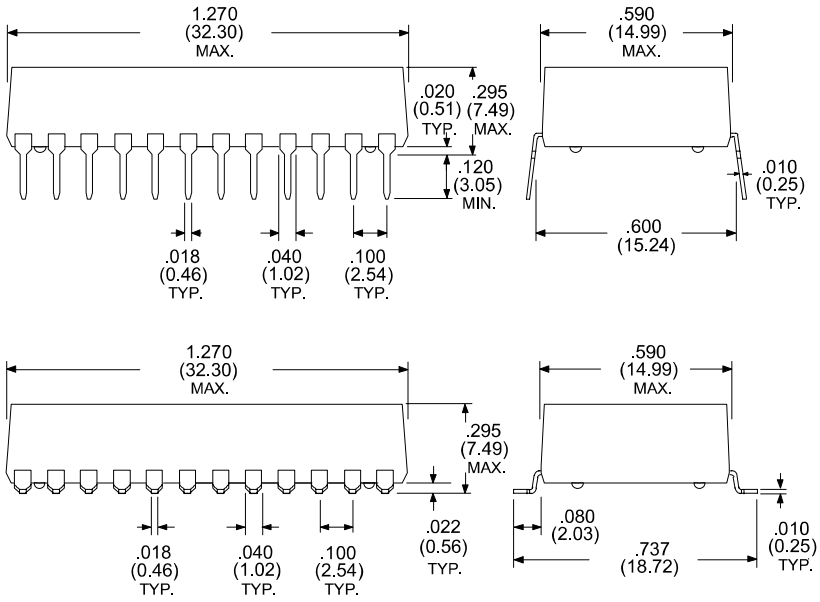


*Alternate Pinout, Similar 20 Tap Electricals, refer to Series **SP24A***

*Also, for same 24-Pin package and Single Output refer to Series **SP24L***

Dimensions in Inches (mm)

Default Thru-hole 24-Pin Package. Example: SP24-105



Gull wing SMD Package Add suffix "G" to P/N. Example: SP24-105G

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SP24L Series 24-Pin Single Output Passive Delay Modules

Optimized for Fastest Rise times and Lowest DCR in single configuration

- *Fast Rise Time, Low DCR*
- *Better than 10/1 Td/tr typical*
- *High Bandwidth* $\approx 0.35 / t_r$
- *Low Distortion LC Network*
- *Standard Impedances: 50 - 75 - 100 Ω*
- *Stable Delay vs. Temperature: 100 ppm/°C*
- *Operating Temperature Range -55°C to +125°C*

Operating Specifications - *Passive Delay Lines*

Pulse Overshoot (Pos)	5% to 10%, typical
Pulse Distortion (S)	3% typical
Working Voltage	25 VDC maximum
Dielectric Strength	100VDC minimum
Insulation Resistance	1,000 MΩ min. @ 100VDC
Temperature Coefficient	70 ppm/°C, typical
Bandwidth (f_C)	0.35/t_r approx.
Operating Temperature Range	-55° to +125°C
Storage Temperature Range	-65° to +150°C

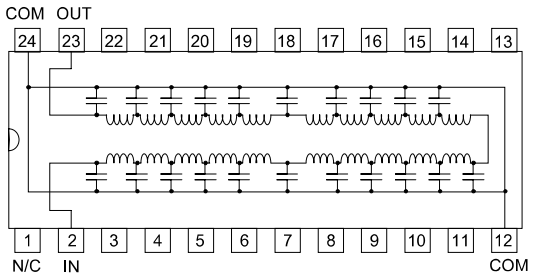
Electrical Specifications [1, 2, 3] at 25°C *Note: For SMD Package Add "G" to end of P/N in Table Below*

Delay (ns)	50 Ohm Part Number	Rise Time max. (ns)	DCR max. (Ohms)	75 Ohm Part Number	Rise Time max. (ns)	DCR max. (Ohms)	100 Ohm Part Number	Rise Time max. (ns)	DCR max. (Ohms)
50 ± 2.50	SP24L-505	5.2	1.5	SP24L-507	5.2	1.8	SP24L-501	5.2	2.0
75 ± 3.75	SP24L-755	7.1	1.9	SP24L-757	7.1	2.2	SP24L-751	7.3	2.3
100 ± 5.00	SP24L1005	9.2	2.4	SP24L1007	9.3	2.6	SP24L1001	9.4	2.6
150 ± 7.50	SP24L1505	13.8	2.5	SP24L1507	14.0	2.7	SP24L1501	14.0	2.7
200 ± 10.0	SP24L2005	16.5	2.6	SP24L2007	16.5	2.9	SP24L2001	16.5	2.9
250 ± 12.5	SP24L2505	22.0	2.9	SP24L2507	22.0	3.4	SP24L2501	22.0	3.5
300 ± 15.0	SP24L3005	22.4	3.1	SP24L3007	22.6	3.7	SP24L3001	22.8	3.9
400 ± 20.0	SP24L4005	34.0	3.8	SP24L4007	35.0	4.8	SP24L4001	36.0	4.9
500 ± 25.0	SP24L5005	42.0	4.8	SP24L5007	42.0	5.8	SP24L5001	42.0	6.2
750 ± 37.5	SP24L7505	69.0	6.4	SP24L7507	69.0	7.1	SP24L7501	69.0	7.2
1000 ± 50.0	SP24L10005	94.0	7.2	SP24L10007	94.0	8.8	SP24L10001	94.0	9.6
1200 ± 60.0	SP24L12005	110.0	8.3	SP24L12007	111.0	9.8	SP24L12001	112.0	10.4

1. Rise Times are measured from 10% to 90% points.
2. Delay Times measured at 50% points of leading edge.
3. Output (100% Tap) terminated to ground through $R_L = Z_O$

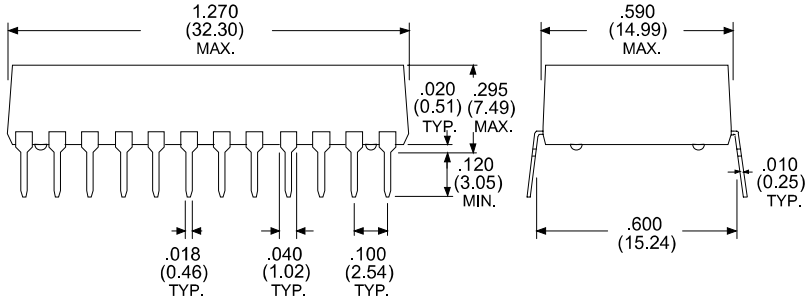
RoHS Version add suffix "R": SP24L-507R

SP24L Style Single Output Schematic



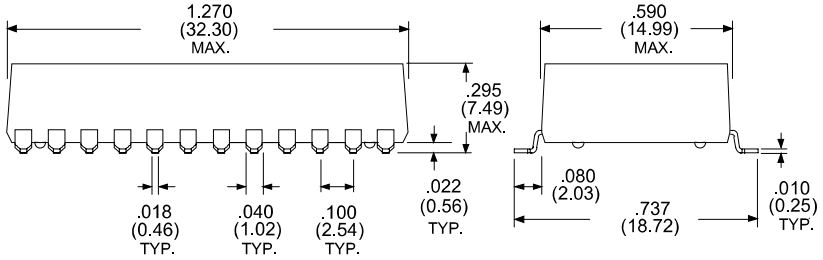
Dimensions in Inches (mm)

Default Thru-hole 24-Pin Package Example: SP24L1001



For similar package, alternate schematic style with only one common connection (pin 24 = N/C) at pin 12, refer to Series ***SP241***

For 20 Tap versions in the same 24-Pin package, refer to Series ***SP24A*** *&* ***SP24A***



Gull wing SMD Package Add suffix "G" to P/N. Example: SP24L1001G

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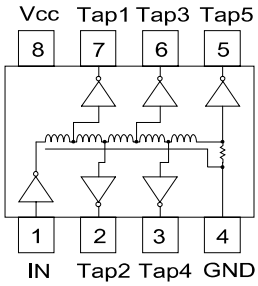
FAMDM Series FAST / TTL Buffered 5-Tap Delay Modules

- *Low Profile 8-Pin Package*
  Two Surface Mount Versions
- *FAST/TTL Logic Buffered*
- *5 Equal Delay Taps*
- *Operating Temperature*
  Range 0°C to +70°C
- *14-Pin Versions: FAMDM Series*
  SIP Versions: FSIDM Series
- *Low Voltage CMOS Versions*
  refer to LVMDM / LVIDM Series

FAMDM 8-Pin Schematic



Electrical Specifications at 25°C

FAST 5 Tap 8-Pin DIP P/N	Tap Delay Tolerances +/- 5% or 2ns (+/- 1ns <13ns)					Tap-to-Tap (ns)
	Tap 1	Tap 2	Tap 3	Tap 4	Total - Tap 5	
FAMDM-7	3.0	4.0	5.0	6.0	7 ± 1.0	** 1 ± 0.5
FAMDM-9	3.0	4.5	6.0	7.5	9 ± 1.0	** 1.5 ± 0.5
FAMDM-11	3.0	5.0	7.0	9.0	11 ± 1.0	** 2 ± 0.7
FAMDM-13	3.0	5.5	8.0	10.5	13 ± 1.5	** 2.5 ± 1.0
FAMDM-15	3.0	6.0	9.0	12.0	15 ± 1.5	3 ± 1.0
FAMDM-20	4.0	8.0	12.0	16.0	20 ± 2.0	4 ± 1.5
FAMDM-25	5.0	10.0	15.0	20.0	25 ± 2.0	5 ± 2.0
FAMDM-30	6.0	12.0	18.0	24.0	30 ± 2.0	6 ± 2.0
FAMDM-35	7.0	14.0	21.0	28.0	35 ± 2.0	7 ± 2.0
FAMDM-40	8.0	16.0	24.0	32.0	40 ± 2.0	8 ± 2.0
FAMDM-50	10.0	20.0	30.0	40.0	50 ± 2.5	10 ± 2.0
FAMDM-60	12.0	24.0	36.0	48.0	60 ± 3.0	12 ± 2.0
FAMDM-75	15.0	30.0	45.0	60.0	75 ± 3.75	15 ± 2.5
FAMDM-100	20.0	40.0	60.0	80.0	100 ± 5.0	20 ± 3.0
FAMDM-125	25.0	50.0	75.0	100.0	125 ± 6.25	25 ± 3.0
FAMDM-150	30.0	60.0	90.0	120.0	150 ± 7.5	30 ± 3.0
FAMDM-200	40.0	80.0	120.0	160.0	200 ± 10.0	40 ± 4.0
FAMDM-250	50.0	100.0	150.0	200.0	250 ± 12.5	50 ± 5.0
FAMDM-350	70.0	140.0	210.0	280.0	350 ± 17.5	70 ± 5.0
FAMDM-500	100.0	200.0	300.0	400.0	500 ± 25.0	100 ± 10.0

** These part numbers do not have 5 equal taps. Tap-to-Tap Delays reference Tap 1.

TEST CONDITIONS -- FAST / TTL

V_{CC} Supply Voltage 5.00VDC
Input Pulse Voltage 3.20V
Input Pulse Rise Time ..... 3.0 ns max.
Input Pulse Width / Period ..... 1000 / 2000 ns

1. Measurements made at 25°C
2. Delay Times measured at 1.50V level of leading edge.
3. Rise Times measured from 0.75V to 2.40V.
4. 10pf probe and fixture load on output under test.

OPERATING SPECIFICATIONS

V_{CC} Supply Voltage ..... 5.00 ± 0.25 VDC
I_{CC} Supply Current ..... 48 mA Maximum
Logic "1" Input: V_{IH} ..... 2.00 V min., 5.50 V max.
I_{IH} ..... 20 µA max. @ 2.70V
Logic "0" Input: V_{IL} ..... 0.80 V max.
I_{IL} ..... -0.6 mA mA
V_{OH} Logic "1" Voltage Out ..... 2.40 V min.
V_{OL} Logic "0" Voltage Out ..... 0.50 V max.
P_{WI} Input Pulse Width ..... 40% of Delay min.
Operating Temperature Range ..... 0° to 70°C
Storage Temperature Range ..... -65° to +150°C

P/N Description

FAMDM - XXX X

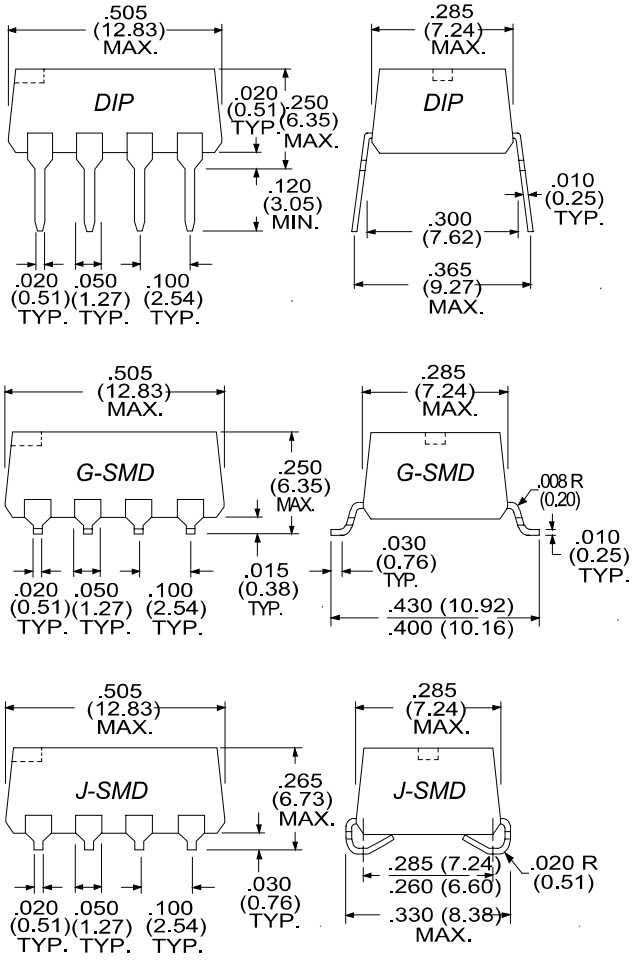
Buffered 5 Tap Delay
Molded Package Series:
8-pin DIP: FAMDM
Total Delay in nanoseconds (ns)
Lead Style: Blank = Thru-hole
G = "Gull Wing" SMD
J = "J" Bend SMD

Examples: FAMDM-25G = 25ns (5ns per tap)
74F, 8-Pin G-SMD

FAMDM-100 = 100ns (20ns per tap)
74F, 8-Pin DIP

RoHS Version add suffix "R": FAMDM-25GR

Dimensions in Inches (mm)



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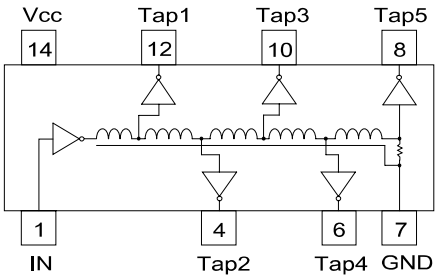
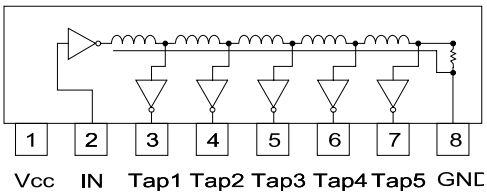
FAIDM / FSIDM Series FAST / TTL Buffered 5-Tap Delay Modules

FAIDM 14-Pin Schematic



FSIDM 8-Pin SIP Schematic



P/N Description ***FXIDM - XXX X***

Logic 5 Tap Delay
Molded Package Series:
14-pin DIP: FAIDM
8-pin SIP: FSIDM
Total Delay in nanoseconds (ns)
Lead Style: Blank = Thru-hole
G = "Gull Wing" SMD *(FAIDM Only)*

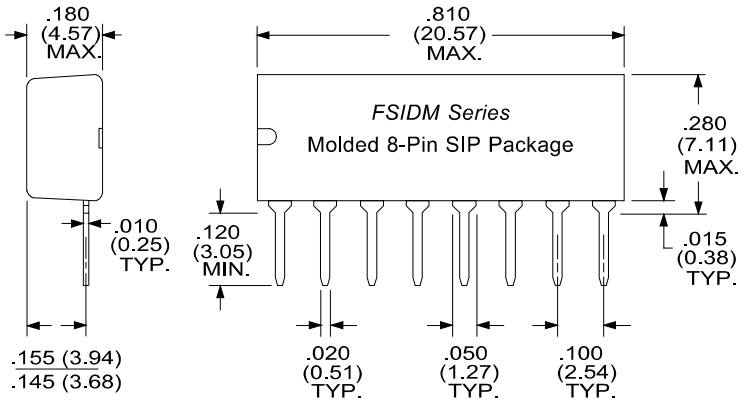
Electrical Specifications at 25°C

74F 5-Tap 14-Pin DIP	*74F 5-Tap 8-Pin SIP*	Tap Delay Tolerances +/- 5% or 2ns					Tap-to-Tap (ns)
		Tap 1	Tap 2	Tap 3	Tap 4	Tap 5	
FAIDM-7	FSIDM-7	3.0	4.0	5.0	6.0	7 ± 1.0	** 1.0 ± 0.4
FAIDM-9	FSIDM-9	3.0	4.5	6.0	7.5	9 ± 1.0	** 1.5 ± 0.5
FAIDM-11	FSIDM-11	3.0	5.0	7.0	9.0	11 ± 1.0	** 2.0 ± 0.7
FAIDM-13	FSIDM-13	3.0	5.5	8.0	10.5	13 ± 1.5	** 2.5 ± 1.0
FAIDM-15	FSIDM-15	3.0	6.0	9.0	12.0	15 ± 1.5	3 ± 1.0
FAIDM-20	FSIDM-20	4.0	8.0	12.0	16.0	20 ± 2.0	4 ± 1.5
FAIDM-25	FSIDM-25	5.0	10.0	15.0	20.0	25 ± 2.0	5 ± 2.0
FAIDM-30	FSIDM-30	6.0	12.0	18.0	24.0	30 ± 2.0	6 ± 2.0
FAIDM-35	FSIDM-35	7.0	14.0	21.0	28.0	35 ± 2.0	7 ± 2.0
FAIDM-40	FSIDM-40	8.0	16.0	24.0	32.0	40 ± 2.0	8 ± 2.0
FAIDM-45	FSIDM-45	9.0	18.0	27.0	36.0	45 ± 2.25	9 ± 2.0
FAIDM-50	FSIDM-50	10.0	20.0	30.0	40.0	50 ± 2.50	10 ± 2.0
FAIDM-60	FSIDM-60	12.0	24.0	36.0	48.0	60 ± 3.0	12 ± 2.0
FAIDM-75	FSIDM-75	15.0	30.0	45.0	60.0	75 ± 3.75	15 ± 2.5
FAIDM-80	FSIDM-80	16.0	32.0	48.0	64.0	80 ± 4.0	16 ± 2.5
FAIDM-100	FSIDM-100	20.0	40.0	60.0	80.0	100 ± 5.0	20 ± 3.0
FAIDM-125	FSIDM-125	25.0	50.0	75.0	100.0	125 ± 6.25	25 ± 3.0
FAIDM-150	FSIDM-150	30.0	60.0	90.0	120.0	150 ± 7.5	30 ± 3.0
FAIDM-200	FSIDM-200	40.0	80.0	120.0	160.0	200 ± 10.0	40 ± 4.0
FAIDM-250	FSIDM-250	50.0	100.0	150.0	200.0	250 ± 12.5	50 ± 5.0
FAIDM-300	FSIDM-300	60.0	120.0	180.0	240.0	300 ± 15.0	60 ± 6.0
FAIDM-350	FSIDM-350	70.0	140.0	210.0	280.0	350 ± 17.5	70 ± 7.0
FAIDM-400	-----	80.0	160.0	240.0	160.0	400 ± 20.0	80 ± 8.0
FAIDM-500	-----	100.0	200.0	300.0	400.0	500 ± 25.0	100 ± 10

RoHS Version add suffix "R": FAIDM-100GR

Examples: FAIDM-25G = 25ns (5ns / tap) , 14-Pin G-SMD
FSIDM-50R = 50ns (10ns / tap), 8-Pin SIP, RoHS

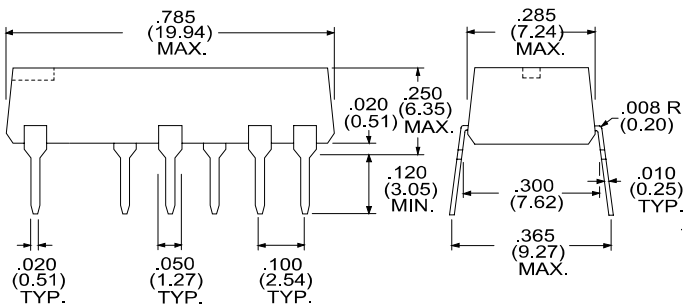
DImensions in Inches (mm)



OPERATING SPECIFICATIONS

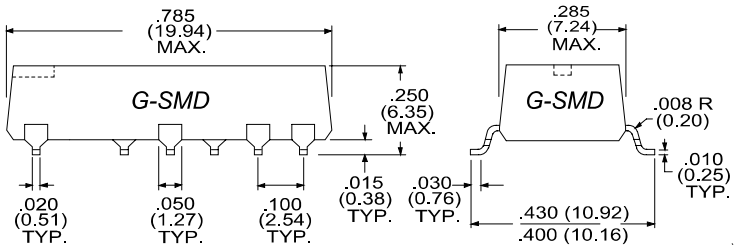
V_{CC} Supply Voltage ..... 5.00 ± 0.25 VDC
I_{CC} Supply Current ..... 48 mA Maximum
Logic "1" Input: V_{IH} ..... 2.00 V min., 5.50 V max.
I_{IH} ..... 20 µA max. @ 2.70V
Logic "0" Input: V_{IL} ..... 0.80 V max.
I_{IL} ..... -0.6 mA mA
V_{OH} Logic "1" Voltage Out ..... 2.40 V min.
V_{OL} Logic "0" Voltage Out ..... 0.50 V max.
P_{WI} Input Pulse Width ..... 40% of Delay min.
Operating Temperature Range ..... 0° to 70°C
Storage Temperature Range ..... -65° to +150°C

FAIDM Series 14-Pin DIP Package



FAIDM Series 14-Pin Gullwing-SMD add "G" suffix to P/N

FAIDM-xxxG

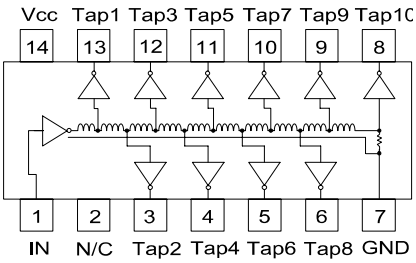


DL22

FAITD Series FAST / TTL Buffered 10-Tap Delay Modules

- *Low Profile 14-Pin Package*
  Two Surface Mount Versions
- *FAST/TTL Logic Buffered*
- *10 Equal Delay Taps*
- *Operating Temperature*
  Range 0°C to +70°C
- *Low Voltage CMOS Versions*
  refer to LVITD Series

FAITD Schematic



Electrical Specifications at 25°C

FAST 10 Tap 14-Pin P/N	Tap Delay Tolerances +/- 5% or 2ns (+/- 1ns <15ns)										Tap-to-Tap (ns)
	Tap 1	Tap 2	Tap 3	Tap 4	Tap 5	Tap 6	Tap 7	Tap 8	Tap 9	Total - Tap 10	
FAITD-12	3	4	5	6	7	8	9	10	11	12 ± 1.0	** 1.0 ± 0.5
FAITD-15	3	3.5	4.5	6	7.5	9	10.5	12	13.5	15 ± 1.0	** 1.5 ± 0.6
FAITD-20	3	4	6	8	10	12	14	16	18	20 ± 1.5	** 2.0 ± 0.7
FAITD-25	3	5	7.5	10	12.5	15	17.5	20	22.5	25 ± 2.0	** 2.5 ± 0.8
FAITD-30	3	6	9	12	15	18	21	24	27	30 ± 2.0	3.0 ± 1.0
FAITD-35	3.5	7	10.5	14	17.5	21	24.5	28	31.5	35 ± 2.0	3.5 ± 1.0
FAITD-40	4	8	12	16	20	24	28	32	36	40 ± 2.0	4.0 ± 1.0
FAITD-50	5	10	15	20	25	30	35	40	45	50 ± 2.5	5.0 ± 2.0
FAITD-60	6	12	18	24	30	36	42	48	54	60 ± 3.0	6.0 ± 2.0
FAITD-70	7	14	21	28	35	42	49	56	63	70 ± 3.5	7.0 ± 2.0
FAITD-75	7.5	15	22.5	30	37.5	45	52.5	60	67.5	75 ± 3.75	7.5 ± 2.0
FAITD-80	8	16	24	32	40	48	56	64	72	80 ± 4.0	8.0 ± 2.0
FAITD-100	10	20	30	40	50	60	70	80	90	100 ± 5.0	10 ± 2.0
FAITD-125	12.5	25	37.5	50	62.5	75	87.5	100	112.5	125 ± 6.25	12.5 ± 3.0
FAITD-150	15	30	45	60	75	90	105	120	135	150 ± 7.5	15 ± 3.0
FAITD-200	20	40	60	80	100	120	140	160	180	200 ± 10.0	20 ± 3.0
FAITD-250	25	50	75	100	125	150	175	200	225	250 ± 12.5	25 ± 3.0
FAITD-300	30	60	90	120	150	180	210	240	270	300 ± 15.0	30 ± 5.0
FAITD-500	50	100	150	200	250	300	350	400	450	500 ± 25.0	50 ± 6.0

** These part numbers do not have 5 equal taps. Tap-to-Tap Delays reference Tap 1.

TEST CONDITIONS -- FAST / TTL

V_{CC} Supply Voltage 5.00VDC
Input Pulse Voltage 3.20V
Input Pulse Rise Time ..... 3.0 ns max.
Input Pulse Width / Period ..... 1000 / 2000 ns

1. Measurements made at 25°C
2. Delay Times measured at 1.50V level of leading edge.
3. Rise Times measured from 0.75V to 2.40V.
4. 10pf probe and fixture load on output under test.

OPERATING SPECIFICATIONS

V_{CC} Supply Voltage ..... 5.00 ± 0.25 VDC
I_{CC} Supply Current ..... 25mA typ., 50 mA Max.
Logic "1" Input: V_{IH} ..... 2.00 V min., 5.50 V max.
I_{IH} ..... 20 μA max. @ 2.70V
Logic "0" Input: V_{IL} ..... 0.80 V max.
I_{IL} ..... -0.6 mA mA
V_{OH} Logic "1" Voltage Out ..... 2.40 V min.
V_{OL} Logic "0" Voltage Out ..... 0.50 V max.
P_{WI} Input Pulse Width ..... 20% of Delay min.
Operating Temperature Range ..... 0° to 70°C
Storage Temperature Range ..... -65° to +150°C

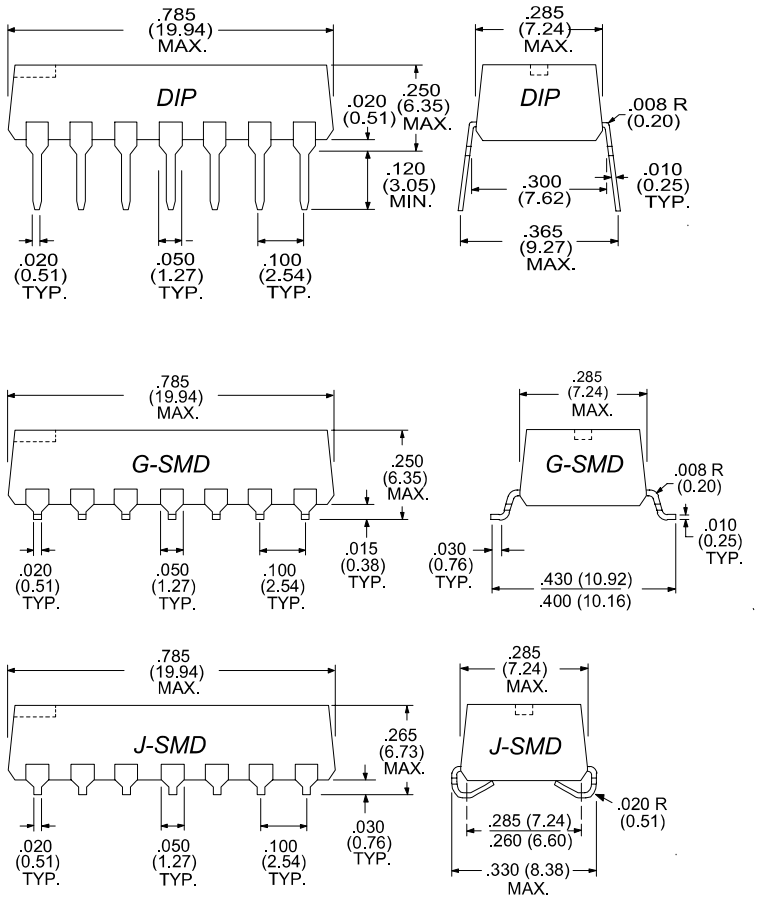
P/N Description ***FAITD - XXX X***

Buffered 10 Tap Delay
Molded Package Series:
14-pin DIP: FAITD
Total Delay in nanoseconds (ns)
Lead Style: Blank = Thru-hole
G = "Gull Wing" SMD
J = "J" Bend SMD

Examples: FAITD-75G = 75ns (7.5ns per tap)
74F, 14-Pin G-SMD
FAITD-100 = 100ns (10ns per tap)
74F, 14-Pin DIP

RoHS Version add suffix "R": FAITD-50R

Dimensions in Inches (mm)



DL22

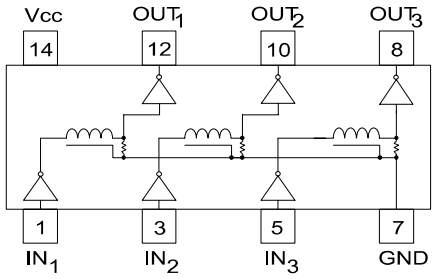
FAST / TTL Logic Buffered Triple & Quad Delays Modules

Uniform or Various Delays in 14-Pin DIP & SMD Packages

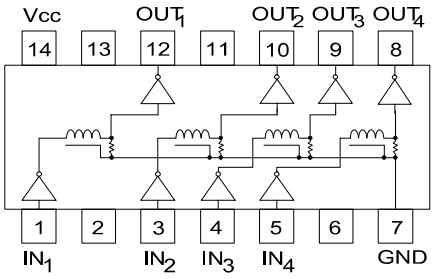
Electrical Specifications at 25°C

Delay (ns)	FAST Buffered Multi-Line	
	Triple P/N	Quadruple P/N
4 ± 1.00	FAI3D-4	FAI4D-4
5 ± 1.00	FAI3D-5	FAI4D-5
6 ± 1.00	FAI3D-6	FAI4D-6
7 ± 1.00	FAI3D-7	FAI4D-7
8 ± 1.00	FAI3D-8	FAI4D-8
10 ± 1.50	FAI3D-10	FAI4D-10
15 ± 2.00	FAI3D-15	FAI4D-15
16 ± 2.00	FAI3D-16	FAI4D-16
20 ± 2.00	FAI3D-20	FAI4D-20
25 ± 2.00	FAI3D-25	FAI4D-25
30 ± 2.00	FAI3D-30	FAI4D-30
50 ± 2.50	FAI3D-50	FAI4D-50

Triple 14-Pin Schematic



Quad 14-Pin Schematic



To Specify G-SMD add "G" suffix to P/N

FAI4D-M Series: Variety of Delays per Part

Refer to Delay tolerances for similar delays above

FAST Logic Multi-Line / Multi-Delay P/N	Line 1 (ns) Pin 1 to Pin 12	Line 2 (ns) Pin 3 to Pin 10	Line 3 (ns) Pin 4 to Pin 9	Line 4 (ns) Pin 5 to Pin 8
FAI4D-M01	4.0	5.0	6.0	7.0
FAI4D-M02	4.0	4.0	8.0	8.0
FAI4D-M03	5.0	5.0	10.0	10.0
FAI4D-M04	4.0	6.0	8.0	10.0
FAI4D-M05	6.0	6.0	12.0	12.0
FAI4D-M06	5.0	7.5	10.0	12.5
FAI4D-M07	7.5	7.5	15.0	15.0
FAI4D-M08	8.0	8.0	16.0	16.0
FAI4D-M09	10.0	10.0	20.0	20.0
FAI4D-M10	5.0	5.0	20.0	20.0
FAI4D-M11	10.0	10.0	20.0	20.0
FAI4D-M12	4.0	8.0	16.0	32.0

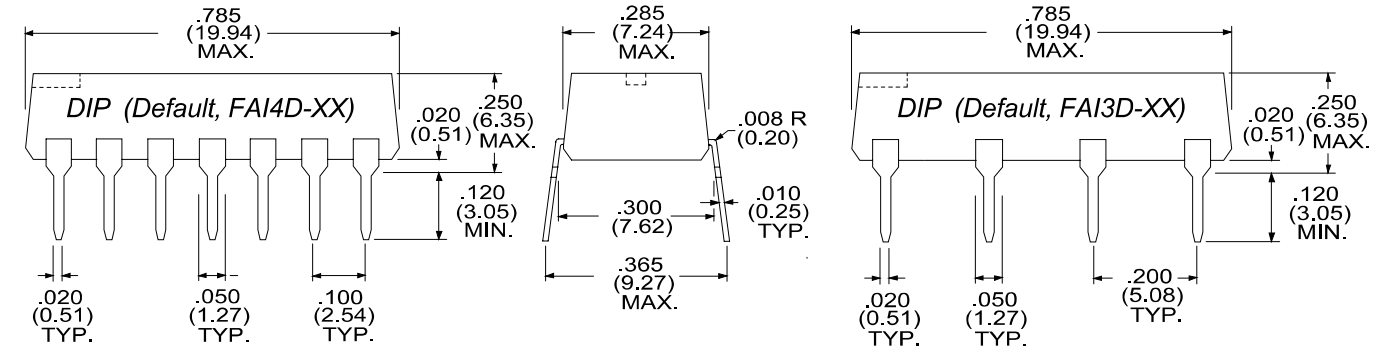
OPERATING SPECIFICATIONS

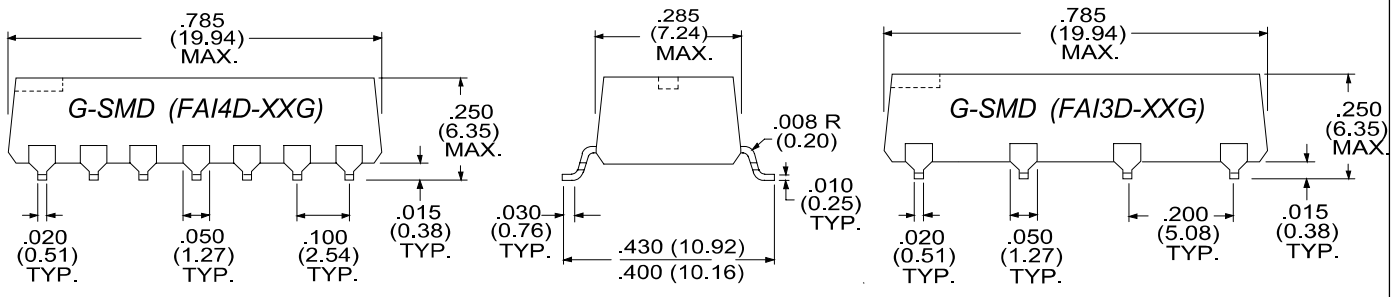
V_{CC} Supply Voltage ..... 5.00 ± 0.25 VDC
I_{CC} Supply Current (3D) ..... 45 mA typ., 95 mA max.
I_{CC} Supply Current (4D) ..... 65 mA typ., 130 mA max.
Logic "1" Input: V_{IH} ..... 2.00 V min., 5.50 V max.
I_{IH} ..... 20 µA max. @ 2.70V
Logic "0" Input: V_{IL} ..... 0.80 V max.
I_{IL} ..... -0.6 mA mA
V_{OH} Logic "1" Voltage Out ..... 2.40 V min.
V_{OL} Logic "0" Voltage Out ..... 0.50 V max.
P_{WI} Input Pulse Width ..... 100% of Delay
Operating Temperature Range ..... 0° to 70°C
Storage Temperature Range ..... -65° to +150°C

TEST CONDITIONS

(Measurements made at 25°C)
V_{CC} Supply Voltage 5.00VDC
Input Pulse Voltage 3.20V
Input Pulse Rise Time ..... 3.0 ns max.
Input Pulse Period ..... 500 ns
Input Pulse Width ..... 1000 ns

Dimensions in Inches (mm)





DL22

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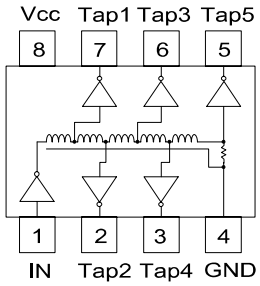
LVMDM Series LVC Low Voltage Logic Buffered 5-Tap Delay SMD Modules

Inputs accept voltages up to 5.5 V

74LVC type input can be driven from either 3.3V or 5V devices. This allows delay module to serve as a translator in a mixed 3.3V / 5V system environment.

- *Low Profile 8-Pin Package Two Surface Mount Versions*
- *Low Voltage CMOS 74LVC Logic Buffered*
- *5 Equal Delay Taps*
- *Operating Temp. -40°C to +85°C*

LVMDM 8-Pin Schematic



Electrical Specifications at 25°C

LVC 5 Tap SMD P/N	Tap 1 (ns)	Tap 2 (ns)	Tap 3 (ns)	Tap 4 (ns)	Tap 5 (ns)	Tap-to-Tap (ns)
LVMDM-7G	3.0 ± 1.0	4.0 ± 1.0	5.0 ± 1.0	6.0 ± 1.0	7 ± 1.0	1.0 ± 0.4
LVMDM-9G	3.0 ± 1.0	4.5 ± 1.0	6.0 ± 1.0	7.5 ± 1.0	9 ± 1.0	1.5 ± 0.5
LVMDM-11G	3.0 ± 1.0	5.0 ± 1.0	7.0 ± 1.0	9.0 ± 1.0	11 ± 1.5	2.0 ± 0.6
LVMDM-13G	3.0 ± 1.0	5.5 ± 1.0	8.0 ± 1.0	10.5 ± 1.0	13 ± 1.5	2.5 ± 0.8
LVMDM-15G	3.0 ± 1.0	6.0 ± 1.0	9.0 ± 1.0	12.0 ± 1.5	15 ± 1.5	3.0 ± 1.0
LVMDM-20G	4.0 ± 1.0	8.0 ± 1.2	12.0 ± 1.5	16.0 ± 1.5	20 ± 2.0	4.0 ± 1.0
LVMDM-25G	5.0 ± 1.0	10.0 ± 1.5	15.0 ± 1.5	20.0 ± 2.0	25 ± 2.0	5.0 ± 1.5
LVMDM-30G	6.0 ± 1.0	12.0 ± 1.5	18.0 ± 1.5	24.0 ± 2.0	30 ± 2.0	6.0 ± 1.5
LVMDM-35G	7.0 ± 1.0	14.0 ± 1.5	21.0 ± 2.0	28.0 ± 2.0	35 ± 2.0	7.0 ± 1.8
LVMDM-40G	8.0 ± 1.0	16.0 ± 1.5	24.0 ± 2.0	32.0 ± 2.0	40 ± 2.0	8.0 ± 2.0
LVMDM-45G	9.0 ± 1.0	18.0 ± 1.5	27.0 ± 2.0	36.0 ± 2.0	45 ± 2.25	9.0 ± 2.0
LVMDM-50G	10.0 ± 1.5	20.0 ± 2.0	30.0 ± 2.0	40.0 ± 2.0	50 ± 2.5	10 ± 2.0
LVMDM-60G	12.0 ± 1.5	24.0 ± 2.0	36.0 ± 2.0	48.0 ± 2.4	60 ± 3.0	12 ± 2.0
LVMDM-75G	15.0 ± 2.0	30.0 ± 2.0	45.0 ± 2.25	60.0 ± 3.0	75 ± 3.75	15 ± 2.5
LVMDM-80G	16.0 ± 2.0	32.0 ± 2.0	48.0 ± 2.4	64.0 ± 3.2	80 ± 4.0	16 ± 2.5
LVMDM-100G	20.0 ± 2.0	40.0 ± 2.0	60.0 ± 3.0	80.0 ± 2.0	100 ± 5.0	20 ± 3.0

** These part numbers do not have 5 equal taps. Tap-to-Tap Delays reference Tap 1.

TEST CONDITIONS -- Low Voltage CMOS, LVC

V_{CC} Supply Voltage 3.30VDC
Input Pulse Voltage 2.70V
Input Pulse Rise Time ..... 3.0 ns max.
Input Pulse Width / Period ..... 1000 / 2000 ns

1. Measurements made at 25°C
2. Delay Times measured at 1.50V level of leading edge.
3. Rise Times measured from 0.75V to 2.40V.
4. 50pf probe and fixture load on output under test.

OPERATING SPECIFICATIONS

Supply Voltage, V_{CC} ..... 3.3 ± 0.3 VDC
Supply Current, I_{CC} ..... 10 mA typ., 30 mA max.
Supply Current, I_{CCL}: V_{IN} = GND ..... 22 mA max.
Supply Current, I_{CCH}: V_{IN} = V_{CC} ..... 10 µA max.
Input Voltage, V_I ..... 0 V min., 5.5 V max.
Logic "1" Input, V_{IH} ..... 2.0 V min.
Logic "0" Input, V_{IL} ..... 0.8 V max.
Logic "1" Out, V_{OH}: V_{CC} = 3V & I_{OH} = -24 mA ..... 2.0 V min.
Logic "0" Out, V_{OL}: V_{CC} = 3V & I_{OL} = 24 mA ..... 0.55 V max.
Input Capacitance, C_I ..... 5 pF, typ.
Input Pulse Width, P_{WI} ..... 40% of Delay min.
Operating Temperature Range ..... -40° to +85°C
Storage Temperature Range ..... -65° to +150°C

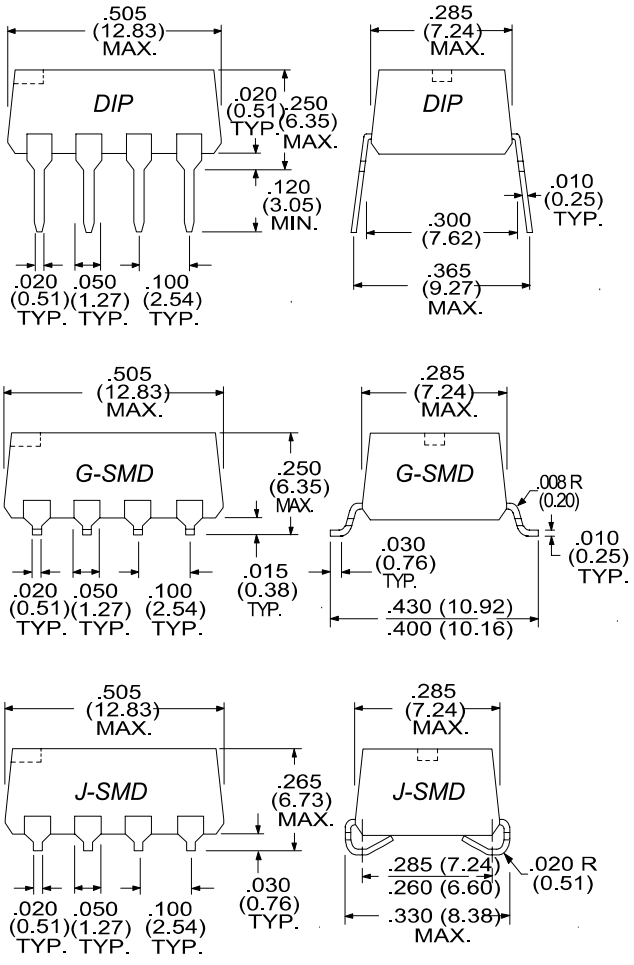
P/N Description *LVMDM - XXX X*

LVC Buffered 5 Tap Delay
Molded Package Series:
8-pin DIP: LVMDM
Total Delay in nanoseconds (ns)
Lead Style: Blank = Thru-hole
G = "Gull Wing" SMD
J = "J" Bend SMD

Examples: LVMDM-25G = 25ns (5ns per tap) 74LVC, 8-Pin G-SMD
LVMDM-100 = 100ns (20ns per tap) 74LVC, 8-Pin DIP

RoHS VersionS add suffix "R": LVMDM-25GR

Dimensions in Inches (mm)



DL22

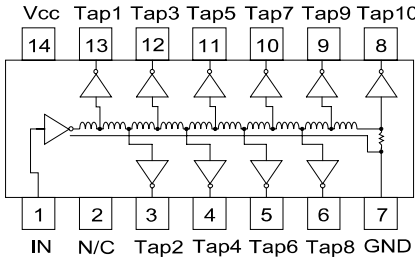
LVITD Series LVC Low Voltage Logic 10-Tap Delay Modules

Inputs accept voltages up to 5.5 V

74LVC type input can be driven from either 3.3V or 5V devices. This allows delay module to serve as a translator in a mixed 3.3V / 5V system environment.

- *Operating Temp. -40°C to +85°C*
- *Low Profile 14-Pin Package*
  Two Surface Mount Versions
- *For 5-Tap 8-Pin Versions see LVMDM Series*

LVITD Schematic



Electrical Specifications at 25°C

LVC Logic 10 Tap P/N	Tap Delay Tolerances +/- 5% or 2ns (>15ns +/- 1.0ns)										Tap-to-Tap (ns)
	Tap 1	Tap 2	Tap 3	Tap 4	Tap 5	Tap 6	Tap 7	Tap 8	Tap 9	Total - Tap 10	
LVITD-12	3	4	5	6	7	8	9	10	11	12 ± 2.5	1.0 ± 0.4
LVITD-21	3	5	7	9	11	13	15	17	19	21 ± 2.5	2.0 ± 0.6
LVITD-30	3	6	9	12	15	18	21	24	27	30 ± 2.5	3.0 ± 0.8
LVITD-50	5	10	15	20	25	30	35	40	45	50 ± 2.5	5.0 ± 1.8
LVITD-60	6	12	18	24	30	36	42	48	54	60 ± 3.0	6.0 ± 2.0
LVITD-75	7.5	15	22.5	30	37.5	45	52.5	60	67.5	75 ± 3.75	7.5 ± 2.0
LVITD-80	8	16	24	32	40	48	56	64	72	80 ± 4.0	8.0 ± 2.0
LVITD-100	10	20	30	40	50	60	70	80	90	100 ± 5.0	10.0 ± 2.0
LVITD-125	12.5	25	37.5	50	62.5	75	87.5	100	112.5	125 ± 6.25	12.5 ± 3.0
LVITD-150	15	30	45	60	75	90	105	120	135	150 ± 7.5	15.0 ± 3.0

TEST CONDITIONS -- Low Voltage CMOS, LVC

V_{CC} Supply Voltage 3.30VDC
Input Pulse Voltage 2.70V
Input Pulse Rise Time ..... 3.0 ns max.
Input Pulse Width / Period ..... 1000 / 2000 ns

1. Measurements made at 25°C
2. Delay Times measured at 1.50V level of leading edge.
3. Rise Times measured from 0.75V to 2.40V.
4. 50pf probe and fixture load on output under test.

OPERATING SPECIFICATIONS

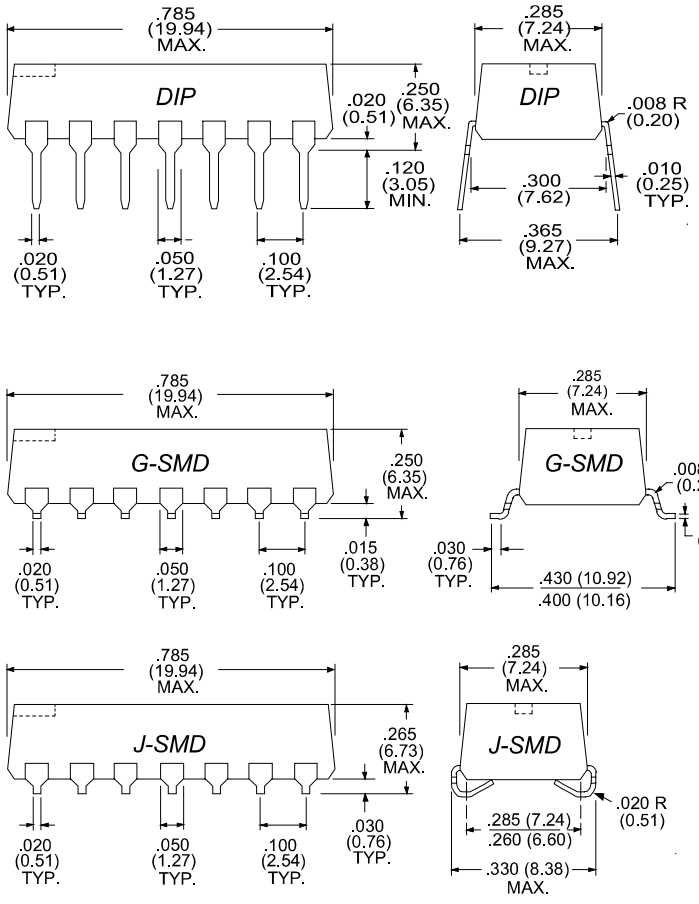
Supply Voltage, V_{CC} ..... 3.3 ± 0.3 VDC
Supply Current, I_{CC} ..... 10 mA typ., 30 mA max.
Supply Current, I_{CCL}: V_{IN} = GND ..... 22 mA max.
Supply Current, I_{CCH}: V_{IN} = V_{CC} ..... 10 µA max.
Input Voltage, V_I ..... 0 V min., 5.5 V max.
Logic "1" Input, V_{IH} ..... 2.0 V min.
Logic "0" Input, V_{IL} ..... 0.8 V max.
Logic "1" Out, V_{OH}: V_{CC} = 3V & I_{OH} = -24 mA ..... 2.0 V min.
Logic "0" Out, V_{OL}: V_{CC} = 3V & I_{OL} = 24 mA ..... 0.55 V max.
Input Capacitance, C_I ..... 5 pF, typ.
Input Pulse Width, P_{WI} ..... 40% of Delay min.
Operating Temperature Range ..... -40° to +85°C
Storage Temperature Range ..... -65° to +150°C

P/N Description *LVITD - XXX X*

LVC Buffered 10 Tap Delay
Molded Package Series:
14-pin DIP: LVITD
Total Delay in nanoseconds (ns)
Lead Style: Blank = Thru-hole
G = "Gull Wing" SMD
J = "J" Bend SMD
R = RoHS

Examples: LVITD-30G = 30ns (3ns per tap) 74LVC, 14-Pin G-SMD
LVITD-100 = 100ns (10ns per tap) 74LVC, 14-Pin DIP

Dimensions in Inches (mm)



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Logic Buffered Single - Dual - Triple Independent Delay Modules

Part Number Description ***XXXXX - XXX X***

74ACT -- ACMDL
ACM2D & ACM3D

74F -- FAMDL
FAM2D & FAM3D

74LVC -- LVMDL
LVM2D & LVM3D

Delay Per Line (ns)

Lead Style:
Blank = Auto-Insertable DIP
G = "Gull Wing" Surface Mount
J = "J" Bend Surface Mount

Examples:
FAMDL-4 = 4ns Single 74F, DIP
ACM2D-25G = 25ns Dual ACT, G-SMD
LVM3D-30G = 30ns Triple LVC, G-SMD

GENERAL: For Operating Specifications and Test Conditions refer to corresponding 5-Tap Series FAMDM, ACMDM and LVMDM except Minimum Pulse width and Supply current ratings as below. Delays specified for the Leading Edge.

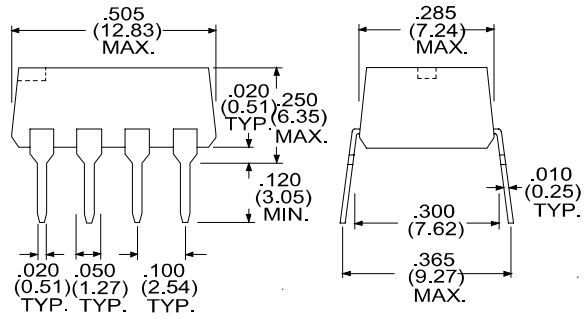
Operating Temperature Range
FAST/TTL ..... 0°C to +70°C
74ACT ..... -40°C to +85°C
74LVC ..... -40°C to +85°C

Temp. Coefficient of Delay:
Single ..... 500ppm/°C typical
Dual/Triple ..... 800ppm/°C typical

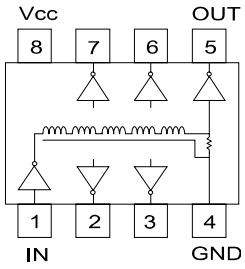
Minimum Input Pulse Width:
Single ..... 40% of total delay
Dual/Triple ..... 100% of total delay

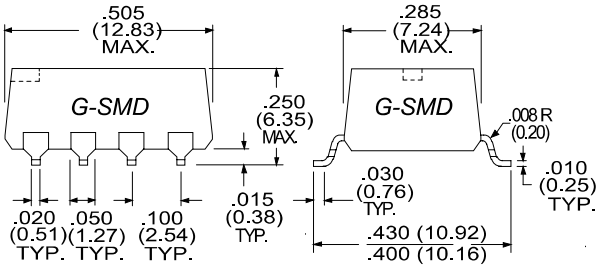
Supply Current, I_{CC} :
FAST/TTL FAMDL ..... 25 mA typ., 48 mA max.
FAM2D ..... 32 mA typ., 65 mA max.
FAM3D ..... 45 mA typ., 95 mA max.
74ACT ACMDL ..... 14 mA typ., 28 mA max.
ACM2D ..... 23 mA typ., 52 mA max.
ACM3D ..... 34 mA typ., 75 mA max.
74LVC LVMDL ..... 10 mA typ., 30 mA max.
LVM2D ..... 15 mA typ., 44 mA max.
LVM3D ..... 21 mA typ., 64 mA max.

Dimensions in Inches (mm)

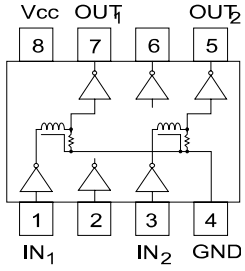


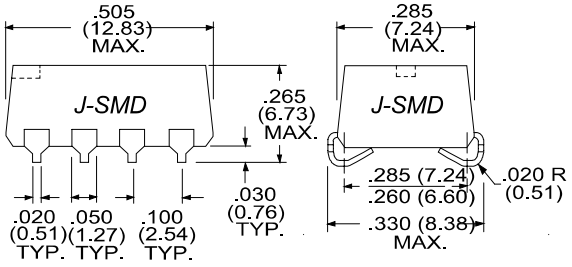
Single 8-Pin "DL" Schematic



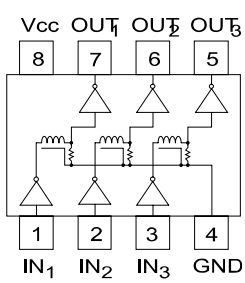


Dual 8-Pin "2D" Schematic





Triple 8-Pin "3D" Schematic



· *FAST / TTL* ·

Electrical Specifications at 25°C

Delay (ns)	FAST Buffered Single 8-Pin P/N	Dual 8-Pin P/N	Triple 8-Pin P/N
4 ± 1.00	FAMDL-4	FAM2D-4	FAM3D-4
5 ± 1.00	FAMDL-5	FAM2D-5	FAM3D-5
6 ± 1.00	FAMDL-6	FAM2D-6	FAM3D-6
7 ± 1.00	FAMDL-7	FAM2D-7	FAM3D-7
8 ± 1.00	FAMDL-8	FAM2D-8	FAM3D-8
9 ± 1.00	FAMDL-9	FAM2D-9	FAM3D-9
10 ± 1.50	FAMDL-10	FAM2D-10	FAM3D-10
12 ± 1.50	FAMDL-12	FAM2D-12	FAM3D-12
15 ± 1.50	FAMDL-15	FAM2D-15	FAM3D-15
16 ± 1.50	FAMDL-16	FAM2D-16	FAM3D-16
20 ± 2.00	FAMDL-20	FAM2D-20	FAM3D-20
25 ± 2.00	FAMDL-25	FAM2D-25	FAM3D-25
30 ± 2.00	FAMDL-30	FAM2D-30	FAM3D-30
50 ± 2.50	FAMDL-50	---	---
75 ± 3.75	FAMDL-75	---	---
100 ± 5.0	FAMDL-100	---	---

· *Advanced CMOS* ·

Electrical Specifications at 25°C

Delay (ns)	74ACT Adv. CMOS Single 8-Pin P/N	Dual 8-Pin P/N	Triple 8-Pin P/N
6 ± 1.00	ACMDL-6	ACM2D-6	ACM3D-6
7 ± 1.00	ACMDL-7	ACM2D-7	ACM3D-7
8 ± 1.00	ACMDL-8	ACM2D-8	ACM3D-8
9 ± 1.00	ACMDL-9	ACM2D-9	ACM3D-9
10 ± 1.50	ACMDL-10	ACM2D-10	ACM3D-10
12 ± 1.50	ACMDL-12	ACM2D-12	ACM3D-12
15 ± 1.50	ACMDL-15	ACM2D-15	ACM3D-15
16 ± 1.50	ACMDL-16	ACM2D-16	ACM3D-16
20 ± 2.00	ACMDL-20	ACM2D-20	ACM3D-20
25 ± 2.00	ACMDL-25	ACM2D-25	ACM3D-25
30 ± 2.00	ACMDL-30	ACM2D-30	ACM3D-30
50 ± 2.50	ACMDL-50	---	---
75 ± 3.75	ACMDL-75	---	---
100 ± 5.0	ACMDL-100	---	---

· *Low Voltage CMOS* ·

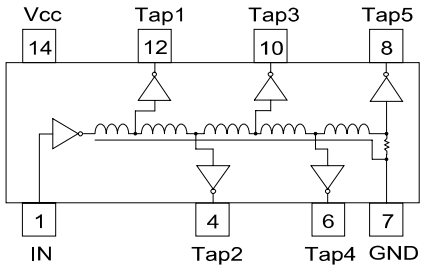
Electrical Specifications at 25°C

Delay (ns)	Low Voltage CMOS Buffered Single 8-Pin P/N	Dual 8-Pin P/N	Triple 8-Pin P/N
4 ± 1.00	LVMDL-4	LVM2D-4	LVM3D-4
5 ± 1.00	LVMDL-5	LVM2D-5	LVM3D-5
6 ± 1.00	LVMDL-6	LVM2D-6	LVM3D-6
7 ± 1.00	LVMDL-7	LVM2D-7	LVM3D-7
8 ± 1.00	LVMDL-8	LVM2D-8	LVM3D-8
9 ± 1.00	LVMDL-9	LVM2D-9	LVM3D-9
10 ± 1.50	LVMDL-10	LVM2D-10	LVM3D-10
12 ± 1.50	LVMDL-12	LVM2D-12	LVM3D-12
15 ± 1.50	LVMDL-15	LVM2D-15	LVM3D-15
16 ± 1.50	LVMDL-16	LVM2D-16	LVM3D-16
20 ± 2.00	LVMDL-20	LVM2D-20	LVM3D-20
25 ± 2.00	LVMDL-25	LVM2D-25	LVM3D-25
30 ± 2.00	LVMDL-30	LVM2D-30	LVM3D-30
50 ± 2.50	LVMDL-50	---	---
75 ± 3.75	LVMDL-75	---	---
100 ± 5.0	LVMDL-100	---	---

DTZM Series FAST / TTL Buffered 5-Tap Delay Modules

- *14-Pin Package Commercial and Mil-Grade Versions*
- *FAST/TTL Logic Buffered*
- *5 Equal Delay Taps*
- *Operating Temperature Ranges 0°C to +70°C, or -55°C to +125°C*
- *8-Pin Versions: FAMDM Series SIP Versions: FSIDM Series*
- *Low Voltage CMOS Versions refer to LVMDM / LVIDM Series*

DTZM 14-Pin Schematic



Electrical Specifications at 25°C

TTL Buffered 5 Tap Modules		Tap Delay Tolerances +/- 5% or 2ns (+/- 1ns <13ns)					Tap-to-Tap (ns)
Part Number	Mil-Grade P/N	Tap 1	Tap 2	Tap 3	Tap 4	Total - Tap 5	
DTZM1-9	DTZM3-9M	5.0	6.0	7.0	8.0	9 ± 1.0	** 1.0 ± 0.5
DTZM1-13	DTZM3-13M	5.0	7.0	9.0	11.0	13 ± 1.5	** 2.0 ± 0.8
DTZM1-17	DTZM3-17M	5.0	8.0	11.0	14.0	17 ± 1.5	3.0 ± 1.0
DTZM1-20	DTZM3-20M	4.0	8.0	12.0	16.0	20 ± 1.5	4.0 ± 1.5
DTZM1-25	DTZM3-25M	5.0	10.0	15.0	20.0	25 ± 2.0	5.0 ± 2.0
DTZM1-30	DTZM3-30M	6.0	12.0	18.0	24.0	30 ± 2.0	6.0 ± 2.0
DTZM1-35	DTZM3-35M	7.0	14.0	21.0	28.0	35 ± 2.0	7.0 ± 2.0
DTZM1-40	DTZM3-40M	8.0	16.0	24.0	32.0	40 ± 2.0	8.0 ± 2.0
DTZM1-45	DTZM3-45M	9.0	18.0	27.0	36.0	45 ± 2.25	9.0 ± 2.0
DTZM1-50	DTZM3-50M	10.0	20.0	30.0	40.0	50 ± 2.5	10 ± 2.0
DTZM1-60	DTZM3-60M	12.0	24.0	36.0	48.0	60 ± 3.0	12 ± 2.0
DTZM1-75	DTZM3-75M	15.0	30.0	45.0	60.0	75 ± 3.75	15 ± 2.5
DTZM1-80	DTZM3-80M	16.0	32.0	48.0	64.0	80 ± 4.0	16 ± 2.5
DTZM1-100	DTZM3-100M	20.0	40.0	60.0	80.0	100 ± 5.0	20 ± 3.0
DTZM1-125	DTZM3-125M	25.0	50.0	75.0	100.0	125 ± 6.25	25 ± 3.0
DTZM1-150	DTZM3-150M	30.0	60.0	90.0	120.0	150 ± 7.5	30 ± 3.0
DTZM1-200	DTZM3-200M	40.0	80.0	120.0	160.0	200 ± 10.0	40 ± 4.0
DTZM1-250	DTZM3-250M	50.0	100.0	150.0	200.0	250 ± 12.5	50 ± 5.0
DTZM1-300	DTZM3-300M	60.0	120.0	180.0	240.0	300 ± 15.0	60 ± 6.0
DTZM1-350	DTZM3-350M	70.0	140.0	210.0	280.0	350 ± 17.5	70 ± 7.0
DTZM1-400	DTZM3-400M	80.0	160.0	240.0	320.0	400 ± 20.0	80 ± 8.0
DTZM1-500	DTZM3-500M	100.0	200.0	300.0	400.0	500 ± 25.0	100 ± 10.0
DTZM1-800	DTZM3-800M	160.0	320.0	480.0	640.0	800 ± 40.0	160 ± 16.0

** These part numbers do not have 5 equal taps. Tap-to-Tap Delays reference Tap 1.

TEST CONDITIONS -- FAST / TTL

V_{CC} Supply Voltage 5.00VDC
Input Pulse Voltage 3.20V
Input Pulse Rise Time ..... 3.0 ns max.
Input Pulse Width / Period ..... 1000 / 2000 ns

1. Measurements made at 25°C
2. Delay Times measured at 1.50V level of leading edge.
3. Rise Times measured from 0.75V to 2.40V.
4. 10pf probe and fixture load on output under test.

OPERATING SPECIFICATIONS

V_{CC} Supply Voltage ..... 5.00 ± 0.25 VDC
I_{CC} Supply Current ..... 48 mA Maximum
Logic "1" Input: V_{IH} ..... 2.00 V min., 5.50 V max.
I_{IH} ..... 20 µA max. @ 2.70V
Logic "0" Input: V_{IL} ..... 0.80 V max.
I_{IL} ..... -0.6 mA mA
V_{OH} Logic "1" Voltage Out ..... 2.40 V min.
V_{OL} Logic "0" Voltage Out ..... 0.50 V max.
P_{WI} Input Pulse Width ..... 40% of Delay min.
Operating Temperature Range ..... 0° to 70°C
Storage Temperature Range ..... -65° to +150°C

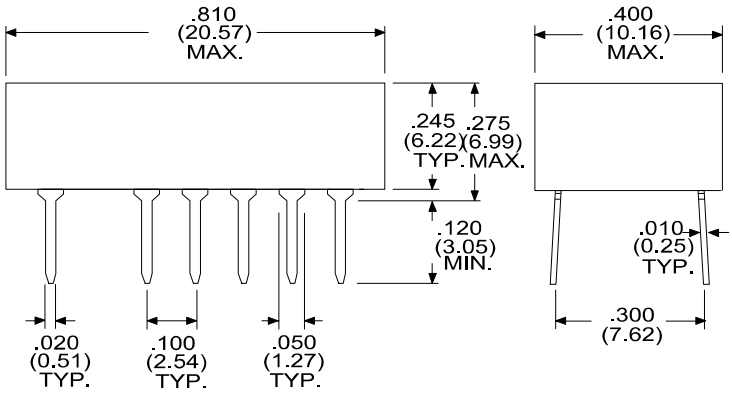
P/N Description ***DTZM1 - XXX X***

Buffered 5 Tap Delays:
14-pin Com'l: DTZM1
14-pin MIL: DTZM3
Total Delay in nanoseconds (ns)
Temp. Range Blank = Commercial
M = Mil-Grade

Examples: DTZM1-25 = 25ns (5ns per tap) 74F, 14-Pin Thru-hole
DTZM3-50M = 50ns (10ns per tap) 74F, 14-Pin, Mil-Grade

Dimensions in Inches (mm)

Commercial Grade 14-Pin Package with Unused Leads Removed as per Schematic. (For Mil-Grade DTZM3 the Height is 0.335")



MIL-GRADE: DTZM3 Military Grade delay lines use integrated circuits screened to MIL-STD-883B with an operating temperature range of -55 to +125°C. These devices have a package height of .335"

Auto-Insertable DIP / Surface Mount Versions, Commercial grade alternates:

Refer to FAIDM Series, same 14-pin footprint, & reduced footprint FAMDM 8-pin Series

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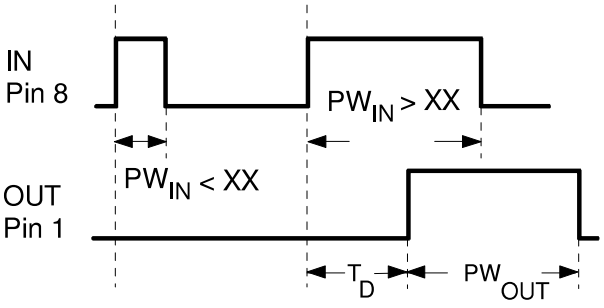
TTLPD Series FAST / TTL Pulse Width Discriminator Modules

- *14-Pin Package Commercial and Mil-Grade Versions*
- *FAST/TTL Logic Buffered*
- *Pass Pulse Widths above & suppress Pulses below Nominal Value*
- *Operating Temperature Ranges 0°C to +70°C, or -55°C to +125°C*



General: Input pulse widths greater than the Nominal value (XX in ns from P/N TTLPD-XX) of the module, will propagate with delay of (XX + 3ns) ± 5% or 2 ns, whichever is greater. Output pulse width will follow the input width ± 7% or 4 ns, whichever is greater. Input pulse widths less than the Nominal value will be suppressed.

TEST CONDITIONS -- FAST / TTL

V_{CC} Supply Voltage 5.00VDC
Input Pulse Voltage 3.20V
Input Pulse Rise Time ..... 3.0 ns max.

1. Measurements made at 25°C
2. Delay / Pulse Widths measured at 1.50V level
3. Rise Times measured from 0.75V to 2.40V.
4. 10pf probe and fixture load on output under test.

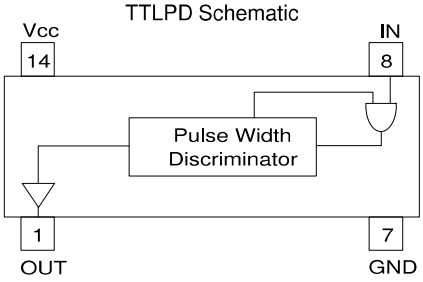
OPERATING SPECIFICATIONS

V_{CC} Supply Voltage ..... 5.00 ± 0.25 VDC
I_{CC} Supply Current ..... 42 mA typ., 60 mA Max.
Logic "1" Input: V_{IH} ..... 2.00 V min., 5.50 V max.
I_{IH} ..... 20 µA max. @ 2.70V
Logic "0" Input: V_{IL} ..... 0.80 V max.
I_{IL} ..... -0.6 mA mA
V_{OH} Logic "1" Voltage Out ..... 2.40 V min.
V_{OL} Logic "0" Voltage Out ..... 0.50 V max.
Operating Temperature Range ..... 0° to 70°C
Storage Temperature Range ..... -65° to +150°C

Electrical Specifications at 25°C

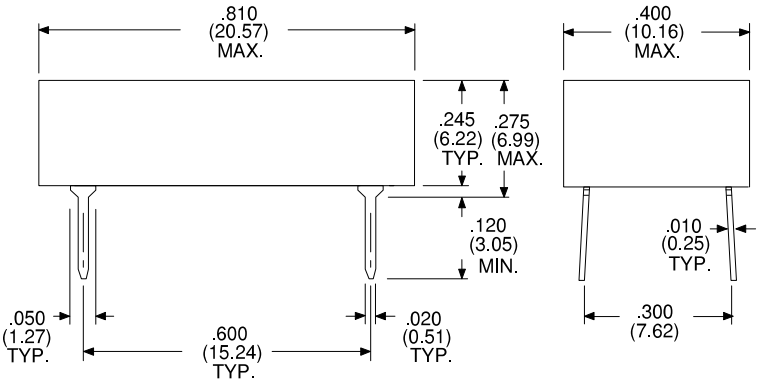
FAST / TTL Pulse Width Discriminator Modules			
Part Number	Mil-Grade Part Number	Suppressed Pulse Width, Max. (ns)	Passed Pulse Width, Min. (ns)
TTLPD-10	TTLPD-10M	< 8.5	> 11.5
TTLPD-15	TTLPD-15M	< 13.5	> 16.5
TTLPD-20	TTLPD-20M	< 18.5	> 21.5
TTLPD-25	TTLPD-25M	< 23.5	> 26.5
TTLPD-30	TTLPD-30M	< 28.5	> 31.5
TTLPD-35	TTLPD-35M	< 33.0	> 37.0
TTLPD-40	TTLPD-40M	< 38.0	> 42.0
TTLPD-50	TTLPD-50M	< 47.5	> 52.5
TTLPD-60	TTLPD-60M	< 57.0	> 63.0
TTLPD-75	TTLPD-75M	< 71.0	> 79.0
TTLPD-80	TTLPD-80M	< 76.0	> 84.0
TTLPD-100	TTLPD-100M	< 95.0	> 105.0
TTLPD-120	TTLPD-120M	< 114.0	> 126.0
TTLPD-125	TTLPD-125M	< 118.7	> 131.3
TTLPD-150	TTLPD-150M	< 142.5	> 157.5
TTLPD-200	TTLPD-200M	< 190.0	> 210.0

TTLPD Schematic



Dimensions in Inches (mm)

Commercial Grade 14-Pin Package with Unused Leads Removed per Schematic. (For Mil-Grade TTLPD-xxxM, Height is 0.335")



MIL-GRADE: These Military Grade devices use integrated circuits screened to MIL-STD-883B with an operating temperature range of -55 to +125°C. These devices have a package height of .335"

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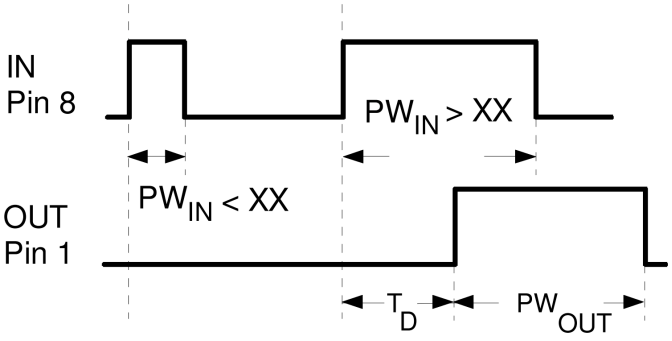
TTLPWG Series FAST / TTL Pulse Width Generator Modules

- *14-Pin Package Commercial and Mil-Grade Versions*
- *FAST/TTL Logic Buffered*
- *Precise Pulse Width Output triggered by Rising Edge of Input*
- *Operating Temperature Ranges 0°C to +70°C, or -55°C to +125°C*



General: Triggered by the input's rising edge (input pulse width 10 ns, min.), a pulse of specified width will be generated at the output with a propagation delay of 4 ± 2 ns (6 ± 2 ns, for inverted output). High-to-low transitions will not trigger the unit. Designed for output duty-cycle less than 50%.

TEST CONDITIONS -- FAST / TTL

V_{CC} Supply Voltage 5.00VDC
Input Pulse Voltage 3.20V
Input Pulse Rise Time ..... 3.0 ns max.
Input Pulse Width / Period ..... 250 / 1000 ns

1. Measurements made at 25°C
2. Delay Times measured at 1.50V level of leading edge.
3. Rise Times measured from 0.75V to 2.40V.
4. 10pf probe and fixture load on output under test.

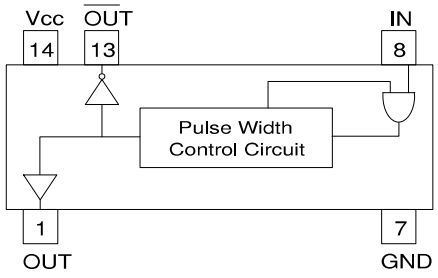
OPERATING SPECIFICATIONS

V_{CC} Supply Voltage ..... 5.00 ± 0.25 VDC
I_{CC} Supply Current ..... 35 mA typ., 55 mA Max.
Logic "1" Input: V_{IH} ..... 2.00 V min., 5.50 V max.
I_{IH} ..... 20 µA max. @ 2.70V
Logic "0" Input: V_{IL} ..... 0.80 V max.
I_{IL} ..... -0.6 mA mA
V_{OH} Logic "1" Voltage Out ..... 2.40 V min.
V_{OL} Logic "0" Voltage Out ..... 0.50 V max.
P_{WI} Input Pulse Width ..... 10 ns min.
Operating Temperature Range ..... 0° to 70°C
Storage Temperature Range ..... -65° to +150°C

Electrical Specifications at 25°C

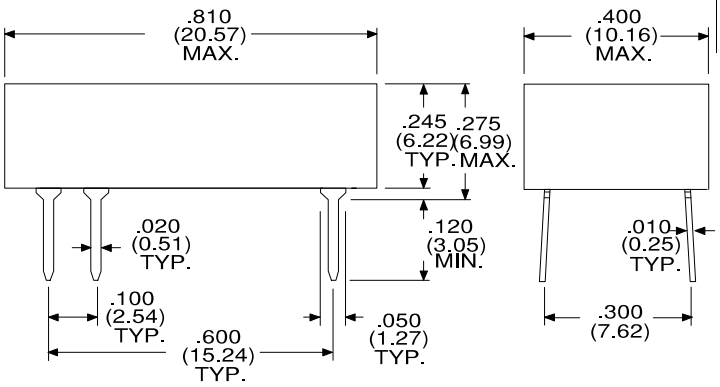
FAST / TTL Buffered Pulse Width Generator Modules			
Part Number	Mil-Grade Part Number	Output Pulse Width (ns)	Maximum Freq. (MHz)
TTLPWG-5	TTLPWG-5M	5 ± 1.0	63
TTLPWG-6	TTLPWG-6M	6 ± 1.0	56
TTLPWG-7	TTLPWG-7M	7 ± 1.0	53
TTLPWG-8	TTLPWG-8M	8 ± 1.0	47
TTLPWG-9	TTLPWG-9M	9 ± 1.0	44
TTLPWG-10	TTLPWG-10M	10 ± 1.5	42
TTLPWG-12	TTLPWG-12M	12 ± 1.5	35
TTLPWG-15	TTLPWG-15M	15 ± 2.0	32
TTLPWG-20	TTLPWG-20M	20 ± 2.0	22
TTLPWG-25	TTLPWG-25M	25 ± 2.0	19
TTLPWG-30	TTLPWG-30M	30 ± 2.0	15
TTLPWG-35	TTLPWG-35M	35 ± 2.0	13
TTLPWG-40	TTLPWG-40M	40 ± 2.0	11
TTLPWG-45	TTLPWG-45M	45 ± 2.25	10
TTLPWG-50	TTLPWG-50M	50 ± 2.5	9
TTLPWG-60	TTLPWG-60M	60 ± 3.0	8
TTLPWG-70	TTLPWG-70M	70 ± 3.5	7
TTLPWG-80	TTLPWG-80M	80 ± 4.0	6
TTLPWG-100	DSP-1348M	100 ± 5.0	5

TTLPWG Schematic



Dimensions in Inches (mm)

Commercial Grade 14-Pin Package with Unused Leads Removed per Schematic. (For Mil-Grade TTLPWG-xxxM, Height is 0.335")



MIL-GRADE: These Military Grade devices use integrated circuits screened to MIL-STD-883B with an operating temperature range of -55 to +125°C. These devices have a package height of .335"

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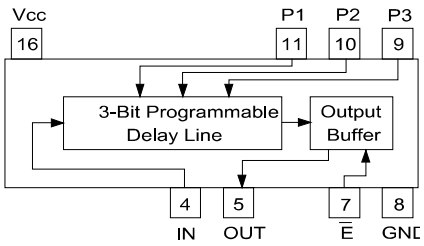
3-Bit Programmable Delay Modules
PLDM4 Series FAST/TTL Logic
7 Delay Steps -- 4 ns Inherent Delay
Available in Surface Mount

FAST/TTL 3-Bit Schematic



Electrical Specifications at 25°C

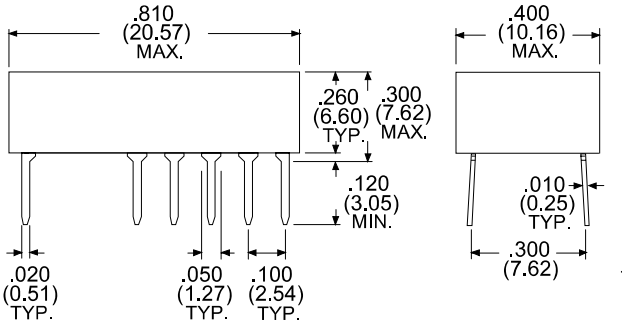
3-Bit FAST Part Number	Delay per Step (ns)	Error ref. to 000 (ns)	Initial Delay (ns)	Referenced to "000" - Delay (ns) per Program Setting (P3*P2*P1)							
			000	000	001	010	011	100	101	110	111
PLDM4-0.5	0.5 ± .25	± .30	4 ± 1.0	0.0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
PLDM4-0.7	0.7 ± .30	± .40	4 ± 1.0	0.0	0.7	1.4	2.1	2.8	3.5	4.2	4.9
PLDM4-0.8	0.8 ± .30	± .50	4 ± 1.0	0.0	0.8	1.6	2.4	3.2	4.0	4.8	5.6
PLDM4-1	1.0 ± .4	± .50	4 ± 1.0	0.0	1.0	2.0	3.0	4.0	5.0	6.0	7.0
PLDM4-1.2	1.2 ± .4	± .60	4 ± 1.0	0.0	1.2	2.4	3.6	4.8	6.0	7.2	8.4
PLDM4-1.25	1.25 ± .5	± .70	4 ± 1.0	0.0	1.25	2.50	3.75	5.00	6.25	7.50	8.75
PLDM4-1.3	1.3 ± .5	± .70	4 ± 1.0	0.0	1.3	2.6	3.9	5.2	6.5	7.8	9.1
PLDM4-1.5	1.5 ± .5	± .70	4 ± 1.0	0.0	1.5	3.0	4.5	6.0	7.5	9.0	10.5
PLDM4-1.8	1.8 ± .6	± .80	4 ± 1.0	0.0	1.8	3.6	5.4	7.2	9.0	10.8	12.6
PLDM4-2	2.0 ± .7	± .80	4 ± 1.0	0.0	2.0	4.0	6.0	8.0	10.0	12.0	14.0
PLDM4-2.5	2.5 ± .7	± .90	4 ± 1.0	0.0	2.5	5.0	7.5	10.0	12.5	15.0	17.5
PLDM4-2.6	2.6 ± .7	± .90	4 ± 1.0	0.0	2.6	5.2	7.8	10.4	13.0	15.6	18.2
PLDM4-3	3.0 ± .7	± 1.0	4 ± 1.0	0.0	3.0	6.0	9.0	12.0	15.0	18.0	21.0

CUMULATIVE TOLERANCES: "Error" Tolerance is for Programmed Delays referenced to Initial Delay, Setting "000."
For example, the setting "111" delay of PLDM4-10 is 70.0 ± 3.0ns ref. to "000," and 74.0 ± 4.0ns referenced to the input.

ENABLE input (Pin 7) is active low. Output will be disabled (low) when " $\overline{E}$ " is high.

INPUT FAN-IN: Input, pin 4, is loaded by the internal passive network and 8 gate inputs (74F type). The source driving Pin 4 should be FAST/TTL (74S/74F) type or equivalent, and should not be used to drive any load other than the delay line input.

Dimensions in Inches (mm)



TEST CONDITIONS -- FAST / TTL

V_{CC} Supply Voltage 5.00VDC
Input Pulse Voltage 3.20V
Input Pulse Rise Time ..... 3.0 ns max.
Input Pulse Width / Period ..... 1000 / 2000 ns

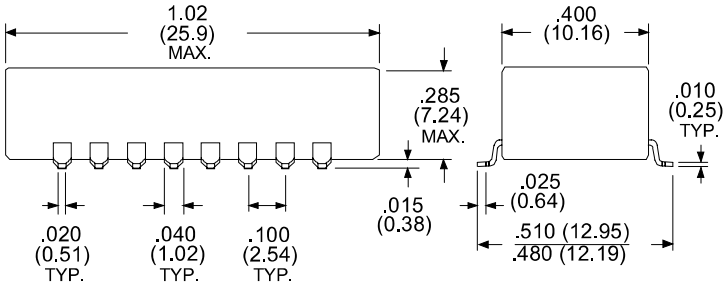
1. Measurements made at 25°C
2. Delay Times measured at 1.50V level of leading edge.
3. Rise Times measured from 0.75V to 2.40V.
4. 10pf probe and fixture load on output.

OPERATING SPECIFICATIONS

V_{CC} Supply Voltage ..... 5.00 ± 0.25 VDC
I_{CC} Supply Current ..... 60 mA typ., 80 mA max
Logic "1" Input *: V_{IH} ..... 2.00 V min., 5.50 V max.
I_{IH} ..... 50 µA max. @ 2.70V
Logic "0" Input *: V_{IL} ..... 0.80 V max.
I_{IL} ..... -0.6 mA mA
V_{OH} Logic "1" Voltage Out ..... 2.40 V min.
V_{OL} Logic "0" Voltage Out ..... 0.50 V max.
P_{WI} Input Pulse Width ..... 40% of Delay min.
Operating Temperature Range ..... -0° to +70°C
Storage Temperature Range ..... -65° to +150°C

* Refer to "INPUT FAN-IN" note above.
IIL/IIH specified for Programming pins 9, 10 & 11.

16-Pin SMD Pkg. Unused leads are NOT removed.
To Specify SMD Package, Add "G" Suffix to P/N
Examples: PLDM4-1.25G, PLDM4-2G



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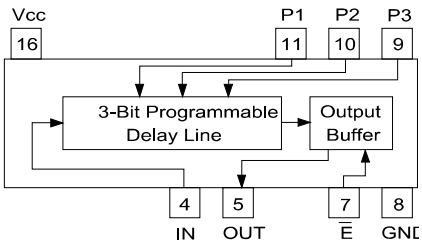
3-Bit Programmable Delay Modules

PLDM7 Series FAST/TTL Logic

7 Delay Steps -- 7 ns Inherent Delay

Available in Surface Mount

FAST/TTL 3-Bit Schematic



Electrical Specifications at 25°C

3-Bit TTL Part Number	Delay per Step (ns)	Error ref. to 000 (ns)	Initial Delay (ns)	Referenced to "000" - Delay (ns) per Program Setting (P3*P2*P1)							
			000	000	001	010	011	100	101	110	111
PLDM7-1	1.0 ± .4	± .50	7 ± 1.0	0.0	1.0	2.0	3.0	4.0	5.0	6.0	7.0
PLDM7-1.2	1.2 ± .4	± .60	7 ± 1.0	0.0	1.2	2.4	3.6	4.8	6.0	7.2	8.4
PLDM7-1.25	1.25 ± .5	± .70	7 ± 1.0	0.0	1.25	2.5	3.75	5.0	6.25	7.5	8.75
PLDM7-1.3	1.3 ± .5	± .70	7 ± 1.0	0.0	1.3	2.6	3.9	5.2	6.5	7.8	9.1
PLDM7-1.5	1.5 ± .5	± .70	7 ± 1.0	0.0	1.5	3.0	4.5	6.0	7.5	9.0	10.5
PLDM7-1.8	1.8 ± .6	± .80	7 ± 1.0	0.0	1.8	3.6	5.4	7.2	9.0	10.8	12.6
PLDM7-1.9	1.9 ± .7	± .80	7 ± 1.0	0.0	1.9	3.8	5.7	7.6	9.5	11.4	13.3
PLDM7-2	2.0 ± .7	± .80	7 ± 1.0	0.0	2.0	4.0	6.0	8.0	10.0	12.0	14.0
PLDM7-2.5	2.5 ± .7	± .90	7 ± 1.0	0.0	2.5	5.0	7.5	10.0	12.5	15.0	17.5
PLDM7-2.6	2.6 ± .7	± .90	7 ± 1.0	0.0	2.6	5.2	7.8	10.4	13.0	15.6	18.2
PLDM7-3	3.0 ± .7	± 1.0	7 ± 1.0	0.0	3.0	6.0	9.0	12.0	15.0	18.0	21.0
PLDM7-5	5.0 ± 1.0	± 1.5	7 ± 1.0	0.0	5.0	10.0	15.0	20.0	25.0	30.0	35.0
PLDM7-8	8.0 ± 1.2	± 2.5	7 ± 1.0	0.0	8.0	16.0	24.0	32.0	40.0	48.0	56.0
PLDM7-10	10.0 ± 1.5	± 3.0	7 ± 1.0	0.0	10.0	20.0	30.0	40.0	50.0	60.0	70.0

CUMULATIVE TOLERANCES: "Error" Tolerance is for Programmed Delays referenced to Initial Delay, Setting "000."
For example, the setting "111" delay of PLDM7-10 is 70.0 ± 3.0ns ref. to "000," and 77.0 ± 4.0ns referenced to the input.

ENABLE input (Pin 7) is active low. Output will be disabled (low) when " $\overline{E}$ " is high.

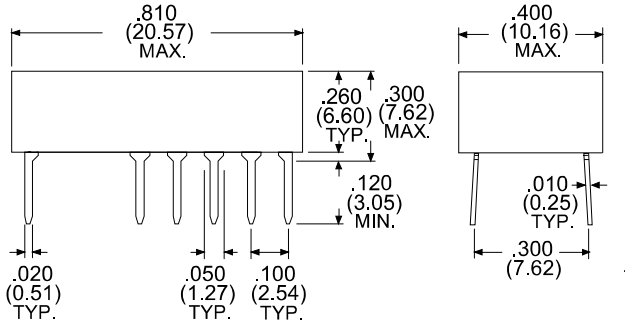
INPUT FAN-IN: Input, pin 4, is loaded by the internal passive network and 8 gate inputs (74S type). The source driving Pin 4 should be FAST/TTL (74S/74F) type or equivalent, and should not be used to drive any load other than the delay line input.

TEST CONDITIONS -- FAST / TTL

V_{CC} Supply Voltage 5.00VDC
Input Pulse Voltage 3.20V
Input Pulse Rise Time ..... 3.0 ns max.
Input Pulse Width / Period ..... 1000 / 2000 ns

1. Measurements made at 25°C
2. Delay Times measured at 1.50V level of leading edge.
3. Rise Times measured from 0.75V to 2.40V.
4. 10pf probe and fixture load on output.

Dimensions in Inches (mm)

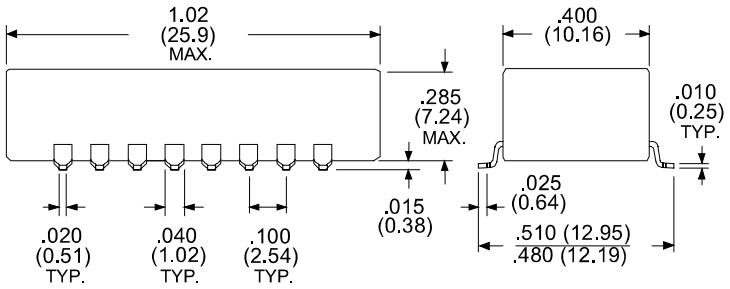


OPERATING SPECIFICATIONS

V_{CC} Supply Voltage ..... 5.00 ± 0.25 VDC
I_{CC} Supply Current ..... 60 mA typ., 80 mA max
Logic "1" Input *: V_{IH} ..... 2.00 V min., 5.50 V max.
I_{IH} ..... 50 µA max. @ 2.70V
Logic "0" Input *: V_{IL} ..... 0.80 V max.
I_{IL} ..... -2.0 mA mA
V_{OH} Logic "1" Voltage Out ..... 2.40 V min.
V_{OL} Logic "0" Voltage Out ..... 0.50 V max.
P_{WI} Input Pulse Width ..... 40% of Delay min.
Operating Temperature Range ..... -0° to +70°C
Storage Temperature Range ..... -65° to +150°C

* Refer to "INPUT FAN-IN" note above.
IIL/IIH specified for Programming pins 9, 10 & 11.

16-Pin SMD Pkg. Unused leads are NOT removed.
To Specify SMD Package, Add "G" Suffix to P/N
Examples: PLDM7-1.25G, PLDM7-2G



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Passive Delay Line Design Considerations

A Passive Delay Line is a special purpose Low Pass Filter designed to delay (phase shift) the input signal by a specified increment of time, and is composed of series inductors and shunt capacitors with values dictated by the line impedance.

Design: This LC network may be used to pass either analog or digital signals whose bandwidth is compatible with the intended range of operation for the delay line. A specific delay and impedance, determine the required LC values of the network:

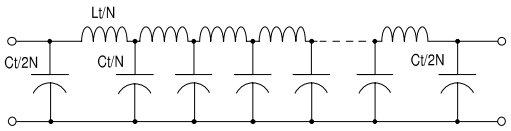


Figure 1A. Passive Delay Line Schematic Diagram.

$$Td = \sqrt{(L_t \times C_t)}$$

$$Z_O = \sqrt{(L_t / C_t)}$$

Td = Total Delay (ns)
Z_O = Impedance (Ohms)
L_t = Total Line Inductance (µH)
C_t = Total Line Capacitance (pF)

Rise Time: The rise time of a delay line is typically measured from the 10% to 90% points of the leading edge of the output pulse. The measured output risetime (t_{ro}) is a function of the input rise time (t_{ri}) and the true rise time of the delay line (t_r):

$$t_r = \sqrt{t_{ro}^2 - t_{ri}^2}$$

An analog delay line's bandwidth (-3dB attenuation) is related to the network's rise time which is dependent upon the total number (N) of LC sections. The delay-to-rise time ratio is the figure of merit, or Quality Factor, used to characterize delay lines. Generally, the greater figure of merit implies higher number of sections, and therefore higher cost. The bandwidth for the network, and number of sections follow these approximations:

$$BW \approx .35 / t_r \qquad N \approx (Td / t_r)^{1.36}$$

Attenuation: The output voltage attenuation of a delay line has several contributing factors:

1. Internal D.C. resistance (DCR)
2. Dielectric and ground plane losses
3. Loading effects at taps
4. Impedance mismatches at terminations
5. Frequency limitations (BW) of delay line

When the delay line is minimally loaded, properly terminated and the input pulse widths are significantly greater than the line's rise time, attenuation is given by:

$$\text{Attenuation (\%)} = 1 - (Zo / (Zo + DCR))$$

Series Connection: Passive delay lines of the same impedance can be connected input-to-output (cascaded) to optimize rise time and/or obtain specific delay values. Termination is required only at the output of the final stage. The rise time of the grouped lines is given by

$$t_{ro} = \sqrt{t_{ri}^2 + t_{r1}^2 + t_{r2}^2 + \ldots t_{rN}^2}$$

Reflections: Loading at taps should be at least 10 times the characteristic impedance to minimize reflections due to transmission line effects. The reflected voltage due to a tap loaded by a resistance, R_L, is given by

$$\text{Reflection (\%)} = 1 - (1 / (1 + Zo/2R_L))$$

In certain applications, mismatches can be used to achieve pulse-shaping requirements.

Reflections, continued: :There are three basic rules relating to reflections in passive delay line applications:

1) No reflections at either terminal of a line which is terminated with its characteristic impedance.

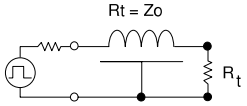


Figure 2A.

2) A reflection, equal in amplitude and of same polarity to the impinging signal, will occur at the input of a line which is open circuited. (R_t = infinite, see figures below.)

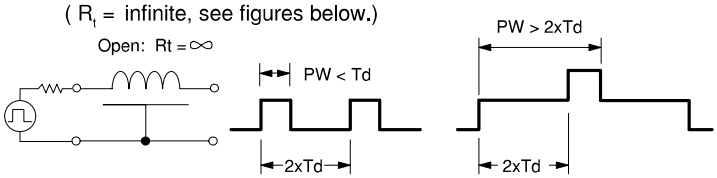


Figure 3A.

3) A reflection, equal in amplitude and of opposite polarity to the impinging signal, will occur at the input of a line which is short circuited. (R_t = 0, see figures below.)

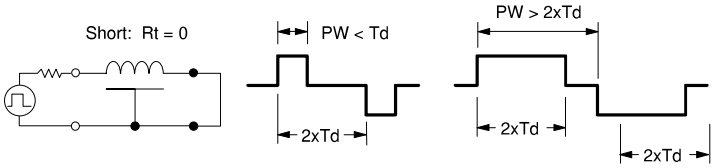


Figure 4A.

Circuit Considerations: To assure delay accuracy and prevent signal distortion, care should be taken to properly integrate the passive delay line into the circuit design. A board trace can load a tap with several picofarads of capacitance which will increase delay, rise time, distortion and attenuation. The designer should calculate inductance and capacitance values of the delay line (L_t , C_t) to determine if anticipated board loading is significant. For typical passive delay line applications, the following design criteria provide optimum performance:

1. The line should be properly terminated.
2. Minimize tap loading. 10 x Z_O min. recommended.
3. Minimize trace lengths to delay line.
4. Circuit should have massive ground plane.
5. All common connections should be used.

We encourage you to call and discuss the details of your design with one of our application engineers. We offer quick turnaround on samples, and custom versions are available, generally at no cost for existing package configurations.

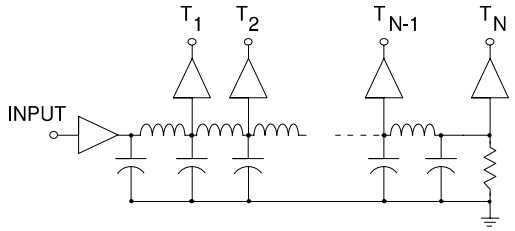
Operating Specifications - *Passive Delay Lines*

Pulse Overshoot (Pos)	5% to 10%, typical
Pulse Distortion (S)	3% typical
Working Voltage	25 VDC maximum
Dielectric Strength	100VDC minimum
Insulation Resistance	1,000 MΩ min. @ 100VDC
Temperature Coefficient	70 ppm/°C, typical
Bandwidth (f_c)	0.35/t_r approx.
Operating Temperature Range	-55° to +125°C
Storage Temperature Range	-65° to +150°C

Logic Buffered Delay Module Design Considerations

- *Delays up to 1000ns*
- *5V -- TTL / FAST, ACT CMOS*
- *3V -- Low Voltage CMOS, LVC, AC*
- *10K & 10KH ECL*
- *5 & 10 Tap Modules*
- *Single / Dual / Triple / Quad*
- *Programmables 3, 4, 5 & 6 Bit*
- *Pulse Width Control*
- *Gated Oscillator Modules*
- *DIP, Gullwing & J Bend SMD*
- *Military Grade Versions Available*
- *Customs available ... Quick Delivery*

General: To avoid the difficulties associated with interfacing passive delay lines with digital integrated circuits, active delay lines have been developed to provide design flexibility and circuit simplification. Logic buffered input and outputs prevent the designer from having to contend with the loading issues of passive circuity, and the related output waveform transients. Unlike a passive delay line whose output rise time is proportional to its delay, the active line's output has the edge rate characteristic of the respective logic family. Similarly, the active delay modules will have the fan-in & fan-out ratings of that logic family. Thus, active delay lines can be used to drive a higher number of gates of a more complicated topology with minimal effect on signal quality or delay accuracy.



Active *Tapped* Delay Line Schematic

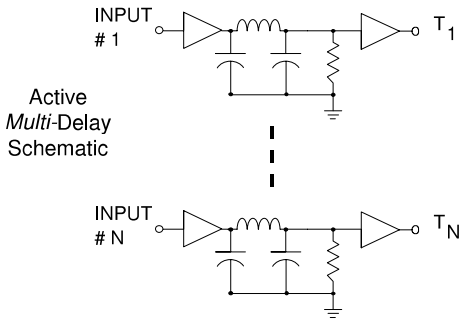
These devices will provide the Digital Design Engineer with simple modular solutions to a variety of timing requirements which commonly arise. Buffered Logic delay modules are ideally suited for situtations where the interval being considered is less than the period of the system clock, or where a precise timing adjustment is required. Also, by incorporating the functions of multiplexers or logic gates, active lines can perform as programmable delays, logic control delays, pulse-width control units and gated oscillators that will, in many applications, be capable of completely replacing complex gate arrangements.

These devices are of hybrid construction, combining Integrated Circuitry with Passive Networks utilizing inductive, capacitive, and resistive elements. Inputs & outputs are internally buffered and compensated for propagation delays and require no external components to perform their intended timing function (for ECL devices standard termination of Open Emitter-Follower Outputs is required).

All modules are designed to meet or exceed all applicable environmental requirements of MIL-D-83532, MIL-STD-883, and MIL-STD-202. Certain families available as MIL-GRADE by adding "M" suffix. Active delay lines are available in a wide variety of standard package configurations, for both through-hole and surface mount applications: "J" Style Surface Mount, Auto Insertable (DIP), Gull Wing Style Surface Mount, and Single-In-Line (SIP).

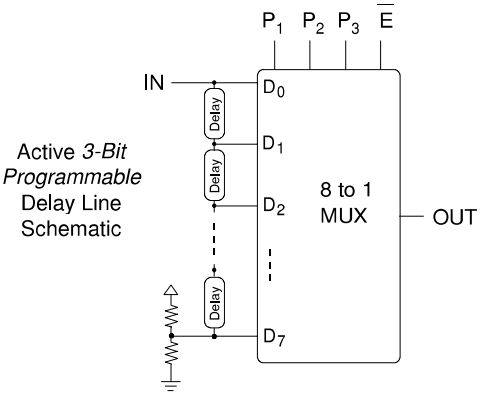
Minimum Pulse Width and BW Limitations: Although the output rise time of an active delay line is characteristic of its logic family, the bandwidth limitation is chiefly due to the rise and fall times of the internal delay network (see Rise time / BW notes for Passive Delays, pg. 2). This Low Pass Filter frequency limitation for active delay lines is expressed as a minimum pulse width that the delay line is guaranteed to pass. Reducing the input pulse width beneath this minimum typically results in shrinking output widths and eventually complete suppression.

Min. PW and BW Limitations, continued: The most significant attenuation occurs at outputs with higher delay. Some degradation of the delay accuracy may occur near these limiting conditions, and we recommend that Delay Modules be evaluated under the intended operating conditions. There are options for increasing the effective bandwidth, and we encourage you to contact us regarding designs where minimum width is an issue.



Active *Multi*-Delay Schematic

Edge-to-Edge Relationship: Typically, active delay lines are specified for leading edge delay accuracy. This is a result of the physical switching properties of integrated circuits. For example, the logic "1" threshold of TTL devices is 2.0 Vdc minimum, at approximately 50% of the margin between the typical TTL low and high levels. However, to reach the TTL logic "0" threshold the negative-going pulse must drop down to 0.8 Vdc, or about 80% of the total signal amplitude. Because of this inherent asymmetry and its effect driving the internal delay circuit, the delay lines output pulse width will typically be less (2 to 3 ns) than the input pulse width. Rhombus has design variations that control delays for Leading and/or Trailing edges, and combinations of pulse polarity, width, and period.



Active *3-Bit Programmable* Delay Line Schematic

Special Requirements: The listings in this catalog are necessarily limited to the most popular versions; intermediate values are readily available, simply contact the factory for data sheets and ordering information. Designs customized to your specific requirements and/or slight modifications to the existing products are welcome. Rhombus customarily provides most engineering services for first article samples at no charge. Please call one of our Applications Engineers today to discuss your requirement.

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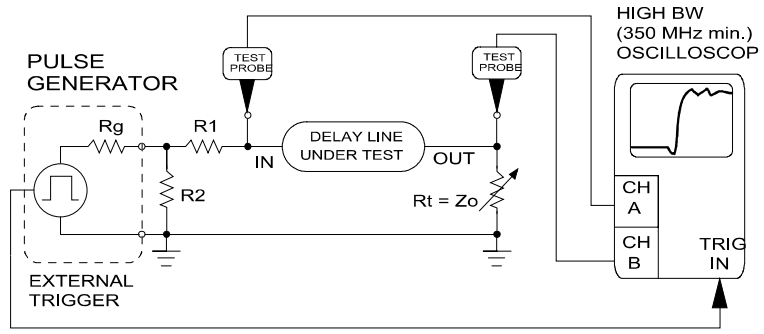
** See Website or Contact Rhombus for details.

Test Circuit & Waveform Parameters



Rg = GENERATOR SOURCE IMPEDANCE = 50 OHMS
R1, R2 = INPUT MATCHING PAD RESISTORS
Rt = TERMINATING RESISTOR
Zo = DELAY LINES CHARACTERISTIC IMPEDANCE

$R1 = \{Rg \times Zo\} / R2$

$R2 = \sqrt{\frac{(Rg^2 \times Zo)}{(Zo - Rg)}}$

Figure 5A. Recommended test circuit for Passive Delay Lines
(For Logic Buffered devices no resistors are required)

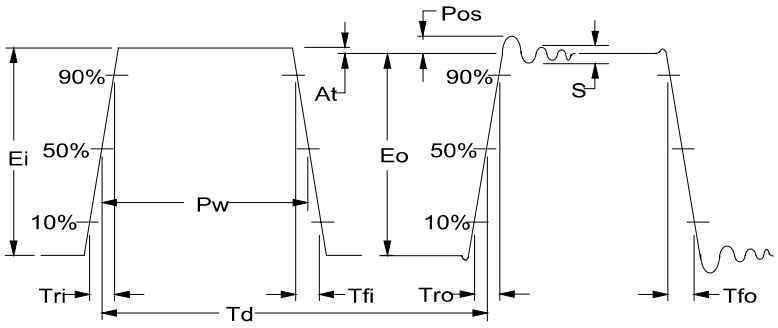


Figure 6A. Passive Delay Line Waveform Parameters

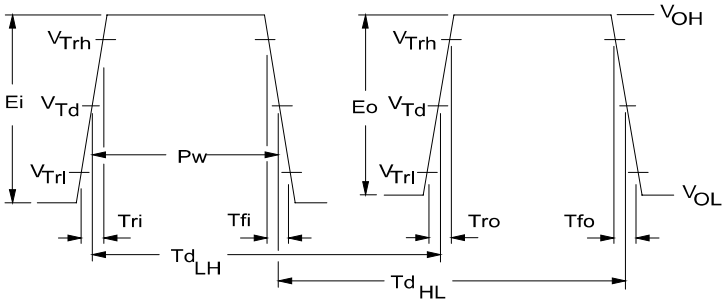


Figure 7A. Active Delay Line Waveform Parameters

Glossary of Delay Line Parameters

Attenuation (At): the difference in peak amplitude between input and output pulses.

D.C. RESISTANCE (DCR): The D.C. resistance, in ohms, measured between the input and output of a delay line.

DELAY TIME (Td): the elapsed time between the respective 50% points on the leading edges of the input and output pulses.

IMPEDANCE (Zo): the effective impedance of the delay line which is equal to the value of the terminating impedance which provides a minimum reflection back to the input of the delay line.

INPUT FALL TIME (Tfi): the elapsed time between the 90% and the 10% points on the trailing edge of the input pulse.

INPUT RISE TIME (Tri): the elapsed time between the 10% and the 90% points on the leading edge of the input pulse.

INPUT VOLTAGE (Ei): the amplitude of the input pulse.

LEADING EDGE: that portion of the pulse which rises from zero to peak amplitude.

OUTPUT RISE TIME (Tfo): the elapsed time between the 10% and the 90% points on the leading edge of the output pulse.

OUTPUT FALL TIME (Tfo): the elapsed time between the 90% and the 10% points on the trailing edge of the output pulse.

OUTPUT VOLTAGE (Eo): the amplitude of the output pulse.

PULSE DISTORTION (S): the magnitude of the largest peak amplitude of all spurious responses in either a positive or negative direction occurring in the period after the top of the leading edge of the output pulse and before two time delays (for flat input pulse top).

PULSE OVERSHOOT (Pos): the peak amplitude of overshoot occurring at the top of the leading edge of the output pulse (for flat input pulse top).

PULSE WIDTH (Pw): the elapsed time between the 50% points on the leading and trailing edge of a pulse.

TRAILING EDGE: that portion of the pulse which falls from peak amplitude to zero.

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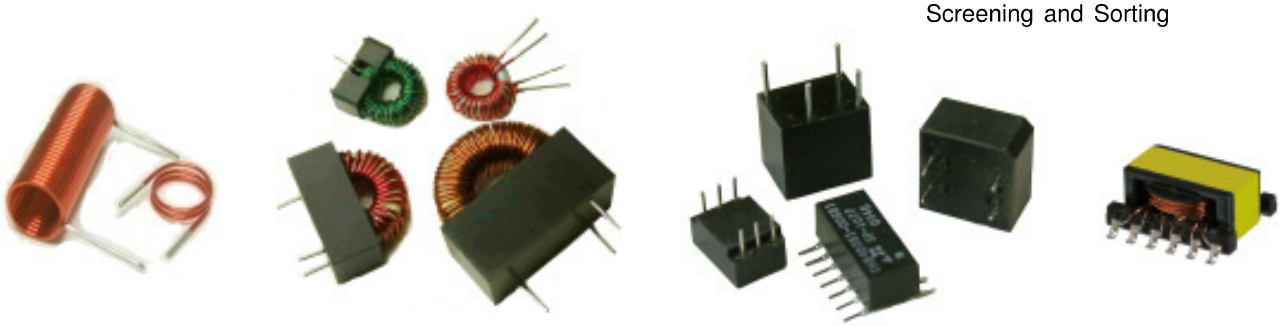

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