Electromagnetic Delay Lines

Total Delays up to 1000ns, Fast Rise Times
Single, 5, 10, 16 & 20 Tap Standard Configurations
Standard Impedances from 50 to 200 Ohms

Ultra Low Attenuation and Distortion
Temperature Stability, 70 ppm/^{O}C Typical.
Operating Temperature Range: 55 to +125^{O}C

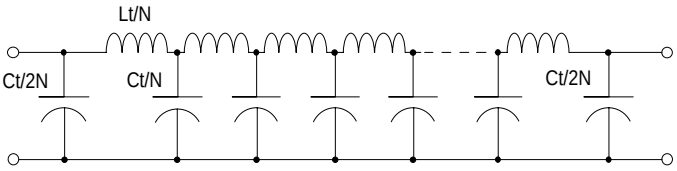
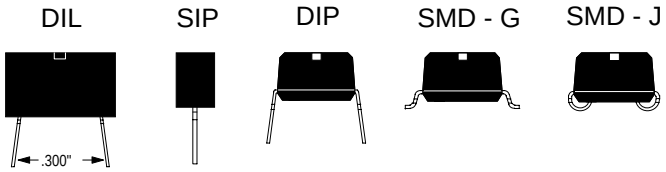


Figure 1A. Passive Delay Line Schematic Diagram.



General: The Passive Delay Modules offered by Rhombus Industries Incorporated have been designed to provide precise delays for use in either analog or digital applications. These lumped constant delay modules offer excellent electrical characteristics with optimal package density. All units exhibit the highest obtainable delay-to-rise-time-ratio (Figure of Merit), are extremely temperature stable, and feature low attenuation and distortion.

These delay modules are offered in standard impedance values of 50, 75, 100 and 200 ohms covering a total delay range of 1ns to 1000ns, and are available in a wide variety of package and pin-out configurations. The most popular delay times and tap tolerances are shown in the tables on the following pages. Temperature coefficient of delay is typically better than +/- 70 ppm/^{O} Centigrade over the recommended operating temperature range of -55 to +125^{O}C. The storage temperature range for all modules is -65 to +150^{O}C.

These Passive Delay Modules are designed to meet or exceed all of the applicable enviornmental requirements of MIL-D-23859, MIL-D-83531 (military general specification for electromagnetic delay lines, which is superseding MIL-D-23859), and MIL-STD-202.

Design: A passive delay line is a special purpose Low Pass Filter composed of series inductors and shunt capacitors used to delay (phase shift) the input signal by a specified increment of time (degrees). This LC network may be used to pass either analog or digital signals whose bandwidth is compatible with the intended range of operation for the delay line. A specific delay and impedance, determine the required LC values of the network:

$$Td = \sqrt{(L_t \times C_t)} \qquad Z_O = \sqrt{(L_t / C_t)}$$

Td = Total Delay (ns)
Z_O = Impedance (Ohms)
L_t = Total Line Inductance (µH)
C_t = Total Line Capacitance (pF)

Rise Time: The rise time of a delay line, is measured from the 10% to 90% points of the leading edge of the output pulse. The measured output risetime (t_{ro}) is a function of the input rise time (t_{ri}) and the true rise time of the delay line (t_r):

$$t_r = \sqrt{t_{ro}^2 - t_{ri}^2}$$

An analog delay line's bandwidth (-3dB attenuation) is related to the network's rise time which is determined by the total number (N) of LC sections. The delay-to-rise time ratio is the figure of merit, or Quality Factor, used to characterize delay lines. Generally, the greater figure of merit implies higher number of sections, and therefore higher cost. The bandwidth for the network, and the number of sections closely follow these approximations:

$$BW = .35 / t_r \qquad N = (Td / t_r)^{1.36}$$

Attenuation: The output voltage attenuation of a delay line has several contributing factors:

1. Internal D.C. resistance (DCR)
2. Dielectric and ground plane losses
3. Loading effects at taps
4. Impedance mismatches at terminations
5. Frequency limitations (BW) of delay line

When the delay line is minimally loaded, properly terminated and the input pulse widths are significantly greater than the line's rise time, attenuation is given by:

$$\text{Attenuation (\%)} = 1 - (Zo / (Zo + DCR))$$

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Reflections: Loading at taps should be at least 10 times the characteristic impedance to minimize reflections due to transmission line effects. The reflected voltage due to a tap loaded by a resistance, R_L, is given by

$$\text{Reflection (\%)} = 1 - (1 / (1 + Zo/2R_L))$$

In certain applications, mismatches can be used to realize pulse-shaping requirements. There are three basic rules relating to reflections:

1) No reflections at either terminal of a line which is terminated with its characteristic impedance. (R_L = Zo)

2) A reflection, equal in amplitude and of same polarity to the impinging signal, will occur at the input of a line which is open circuited. (R_L = infinite, see fig. 2A)

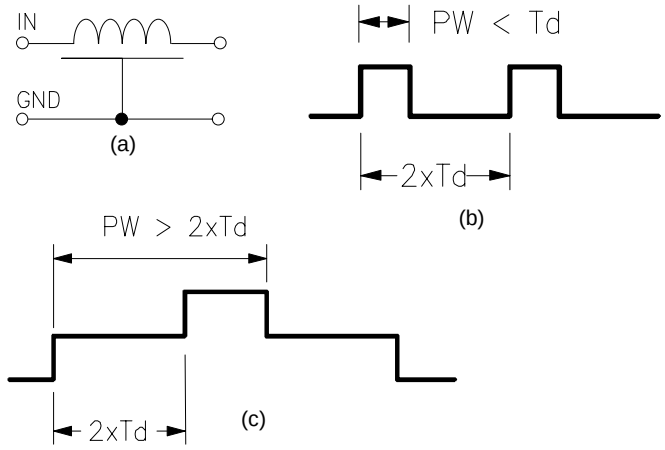

Figure 2A. Output Open circuited (a), and waveforms with reflections at Input for (b) Input Pulse Width < Delay and (c) Input P W > 2 x Delay.

3) A reflection, equal in amplitude and of opposite polarity to the impinging signal, will occur at the input of a line which is short circuited. (R_L = 0, see fig. 3A)

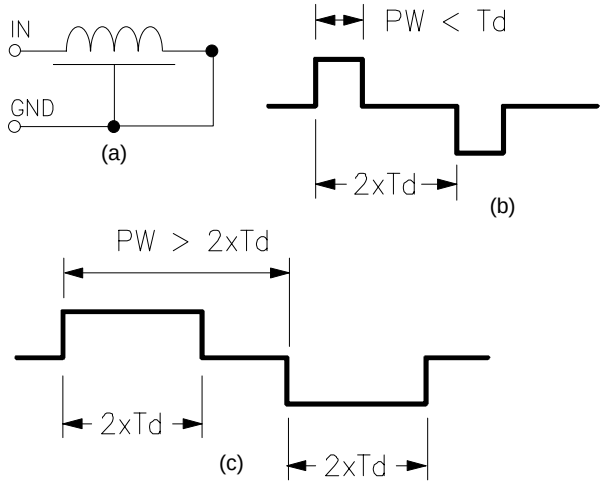

Figure 3A. Output shorted (a), and waveforms with reflections at Input for
(b) Input Pulse Width < Delay and (c) Input P W > 2 x Delay.

Series Connection: Passive delay lines of the same impedance can be connected input-to-output (cascaded) to optimize rise time and/or obtain specific delay values. The rise time of the grouped lines is given by

$$t_{ro} = \sqrt{t_{ri}^2 + t_{r1}^2 + t_{r2}^2 + \ldots t_{rN}^2}$$

The only termination required is at the output of the final stage (See Figure 4A).

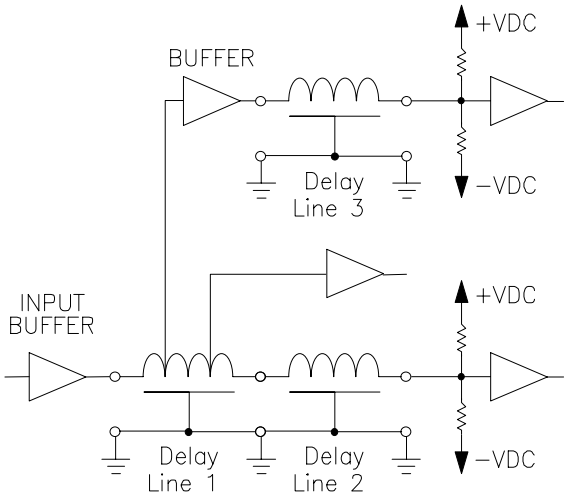

Figure 4A. Example circuit of series implementation. Thevenin style shown; alternate methods of single shunt or series termination may be used as applicable.

Circuit Considerations: To assure delay accuracy and prevent signal distortion, care should be taken to properly integrate the passive delay line into the circuit design. A board trace can load a tap with several picofarads of capacitance which will increase delay, rise time, distortion and attenuation. The designer should calculate inductance and capacitance values (L_t , C_t) of the delay line to determine if anticipated board loading is significant. It is characteristic of higher impedance designs to have higher inductances and lower capacitances, and are thereby more susceptible to loading. For typical passive delay line applications, the following design criteria provide optimum performance:

1. The line should be properly terminated.
2. Minimize tap loading. 10 x Z_O minimum recommended.
3. Minimize trace lengths to delay line.
4. Circuit should have massive ground plane.
5. All common connections should be used.

We encourage you to call and discuss the details of your design with one of our application engineers. We offer quick turnaround on samples, and custom versions are available, generally at no cost for existing package configurations..

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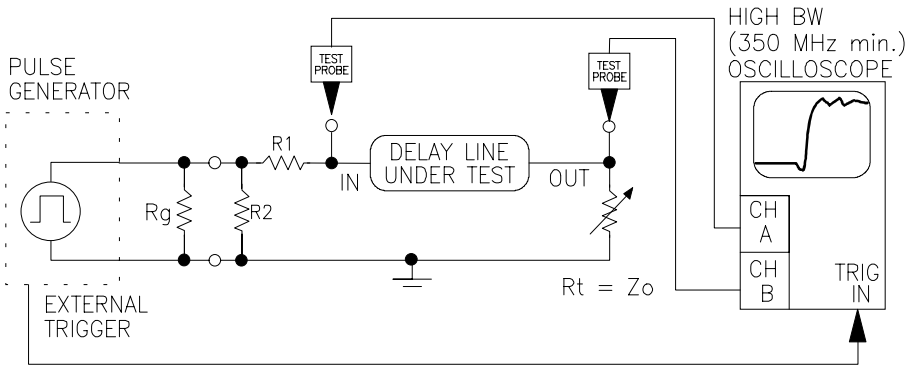

Rg = GENERATOR SOURCE IMPEDANCE = 50 OHMS
R1,R2 = INPUT MATCHING PAD RESISTORS
Rt = TERMINATING RESISTOR
Zo = DELAY LINES CHARACTERISTIC IMPEDANCE

$R1 = \{Rg \times Zo\} / R2$

$R2 = \sqrt{\frac{Rg^2 \times Zo}{Zo - Rg}}$

Figure 5A. Recommended test circuit for Passive Delay Lines

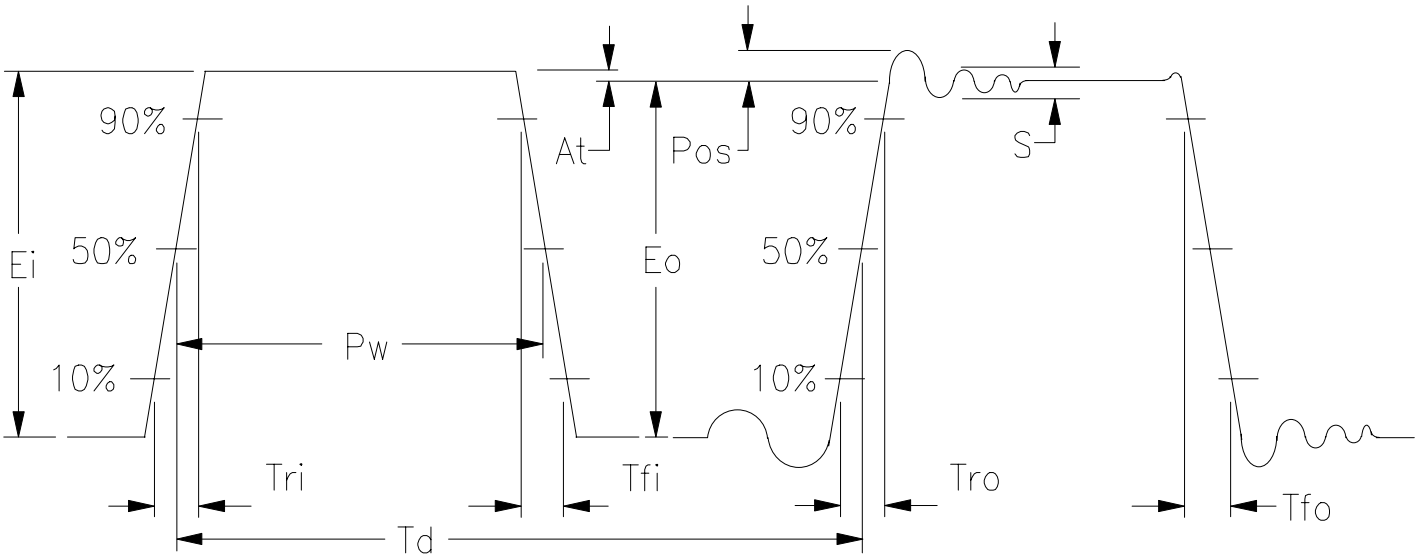

Figure 6A. Passive Delay Line Waveform Parameters

GLOSSARY

LEADING EDGE: that portion of the pulse which rises from zero to peak amplitude.

TRAILING EDGE: that portion of the pulse which falls from peak amplitude to zero.

INPUT VOLTAGE (Ei): the amplitude of the input pulse.

OUTPUT VOLTAGE (Eo): the amplitude of the output pulse.

DELAY TIME (Td): the elapsed time between the respective 50% points on the leading edges of the input and output pulses.

INPUT RISE TIME (Tri): the elapsed time between the 10% and the 90% points on the leading edge of the input pulse.

INPUT FALL TIME (Tfi): the elapsed time between the 90% and the 10% points on the trailing edge of the input pulse.

OUTPUT FALL TIME (Tfo): the elapsed time between the 10% and the 90% points on the leading edge of the output pulse.

OUTPUT FALL TIME (Tfo): the elapsed time between the 90% and the 10% points on the trailing edge of the output pulse.

PULSE WIDTH (Pw): the elapsed time between the 50% points on the leading and trailing edge of a pulse.

PULSE OVERSHOOT (Pos): the peak amplitude of overshoot occurring at the top of the leading edge of the output pulse (for flat input pulse top).

PULSE DISTORTION (S): the magnitude of the largest peak amplitude of all spurious responses in either a positive or negative direction occurring in the period after the top of the leading edge of the output pulse and before two time delays (for flat input pulse top).

IMPEDANCE (Zo): the effective impedance of the delay line which is equal to the value of the terminating impedance which provides a minimum reflection back to the input of the delay line.

D.C. RESISTANCE (DCR): The D.C. resistance, in ohms, measured between the input and output of a delay line.

Attenuation (At): the difference in peak amplitude between input and output pulses.

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